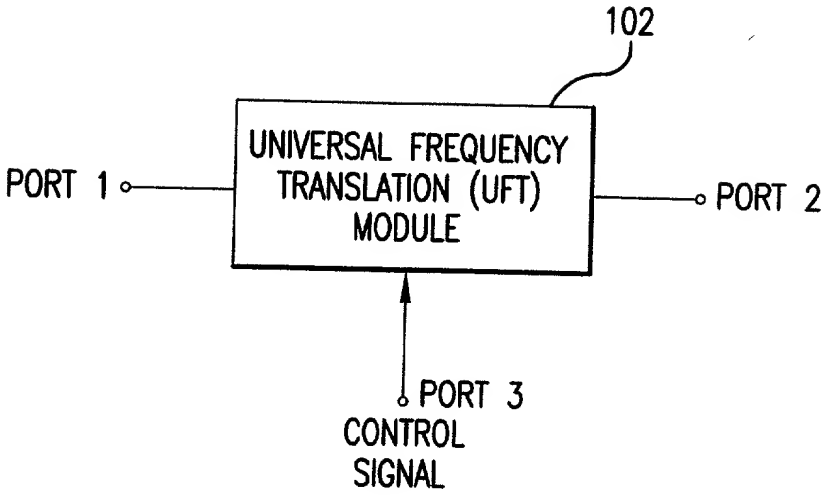
102
UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL

FIG. 1A

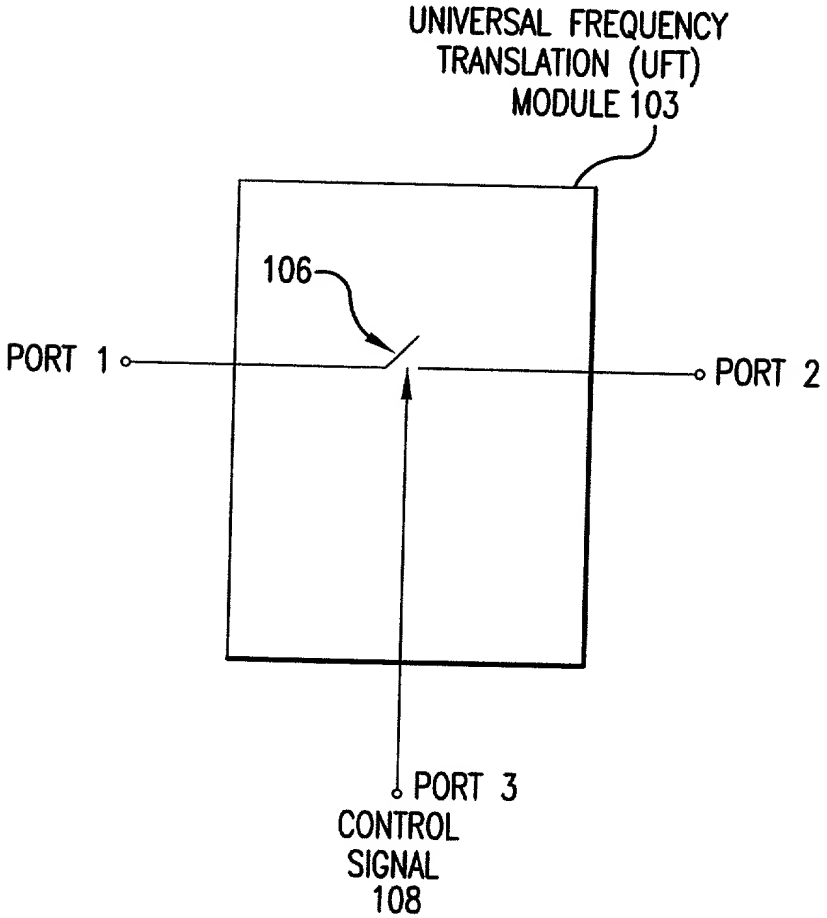
UNIVERSAL FREQUENCY TRANSLATION (UFT) MODULE 103
106
PORT 1
PORT 2
PORT 3
CONTROL SIGNAL 108

FIG. 1B

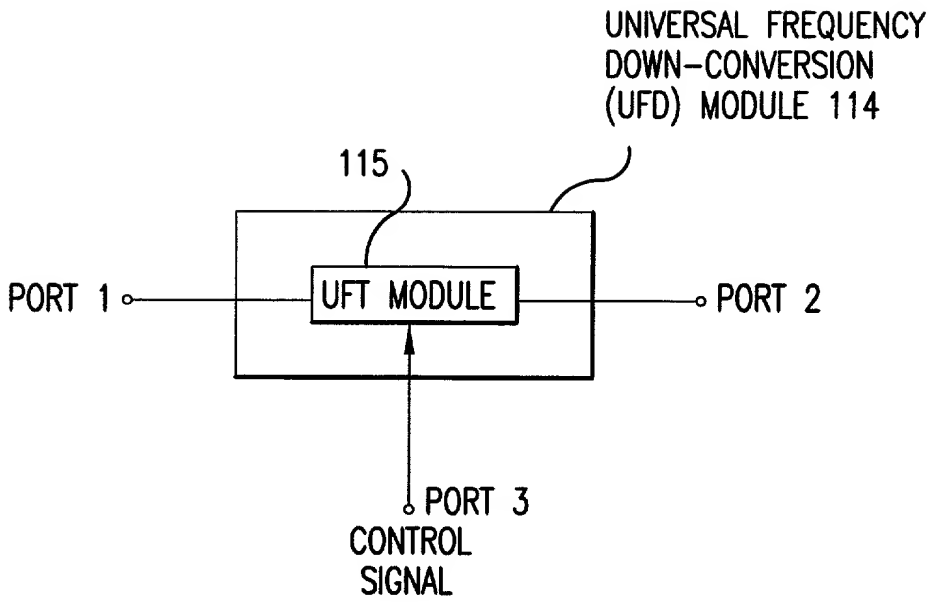
UNIVERSAL FREQUENCY
DOWN-CONVERSION
(UFD) MODULE 114
115
PORT 1
UFT MODULE
PORT 2
PORT 3
CONTROL
SIGNAL

FIG. 1C

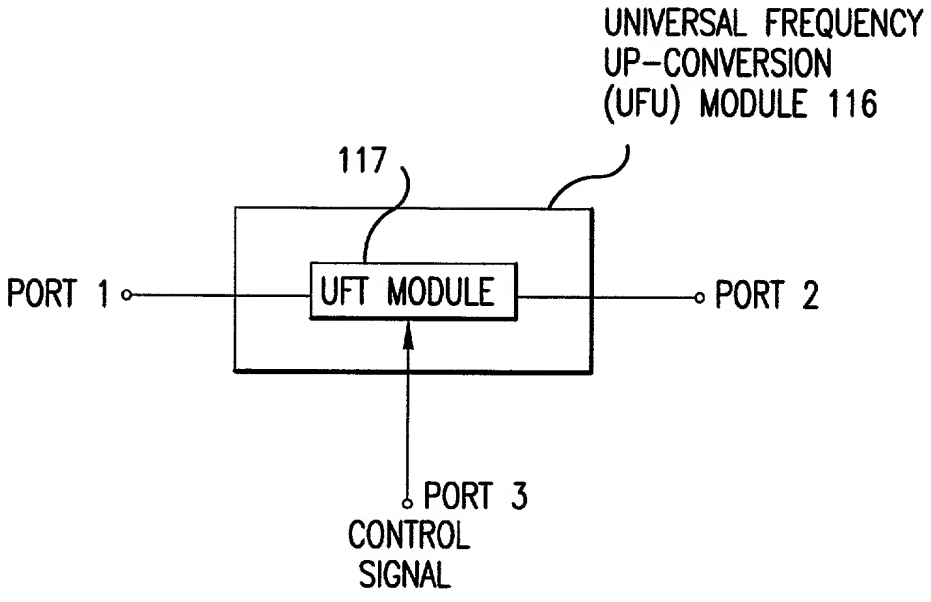
UNIVERSAL FREQUENCY
UP-CONVERSION
(UFU) MODULE 116
117
PORT 1
UFT MODULE
PORT 2
PORT 3
CONTROL
SIGNAL

FIG. 1D

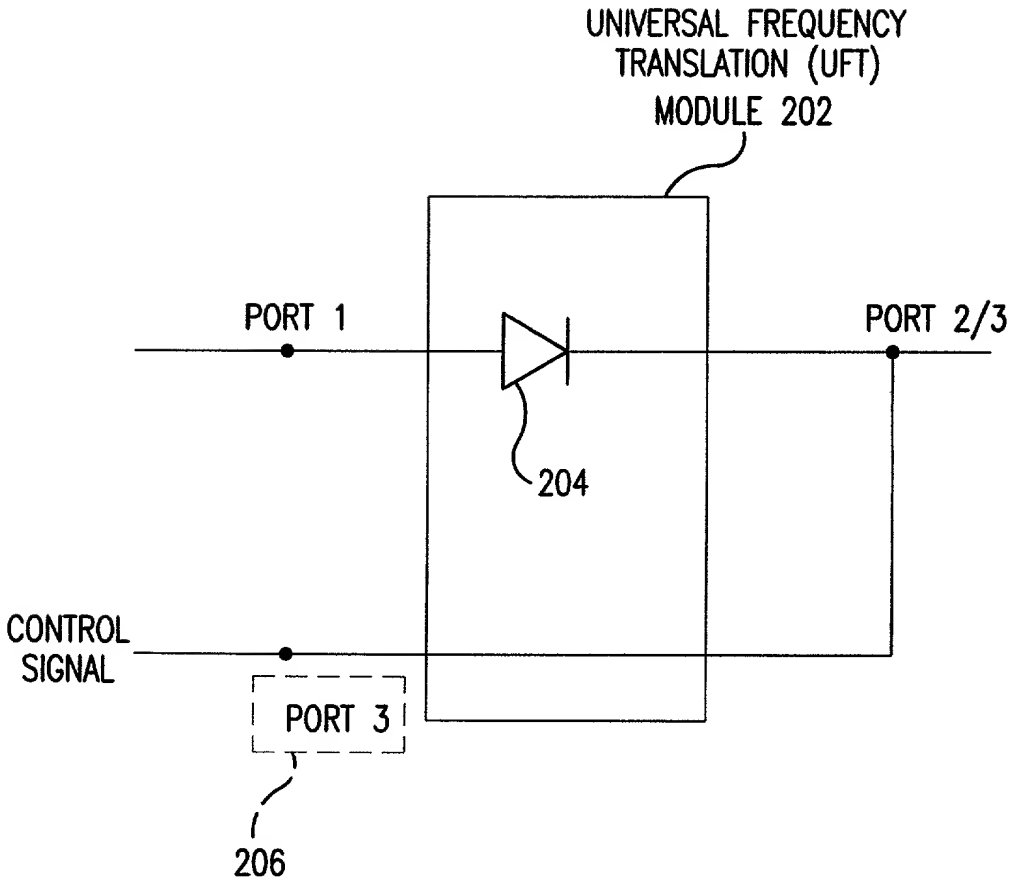
UNIVERSAL FREQUENCY
TRANSLATION (UFT)
MODULE 202
PORT 1
PORT 2/3
204
CONTROL
SIGNAL
PORT 3
206

FIG. 2

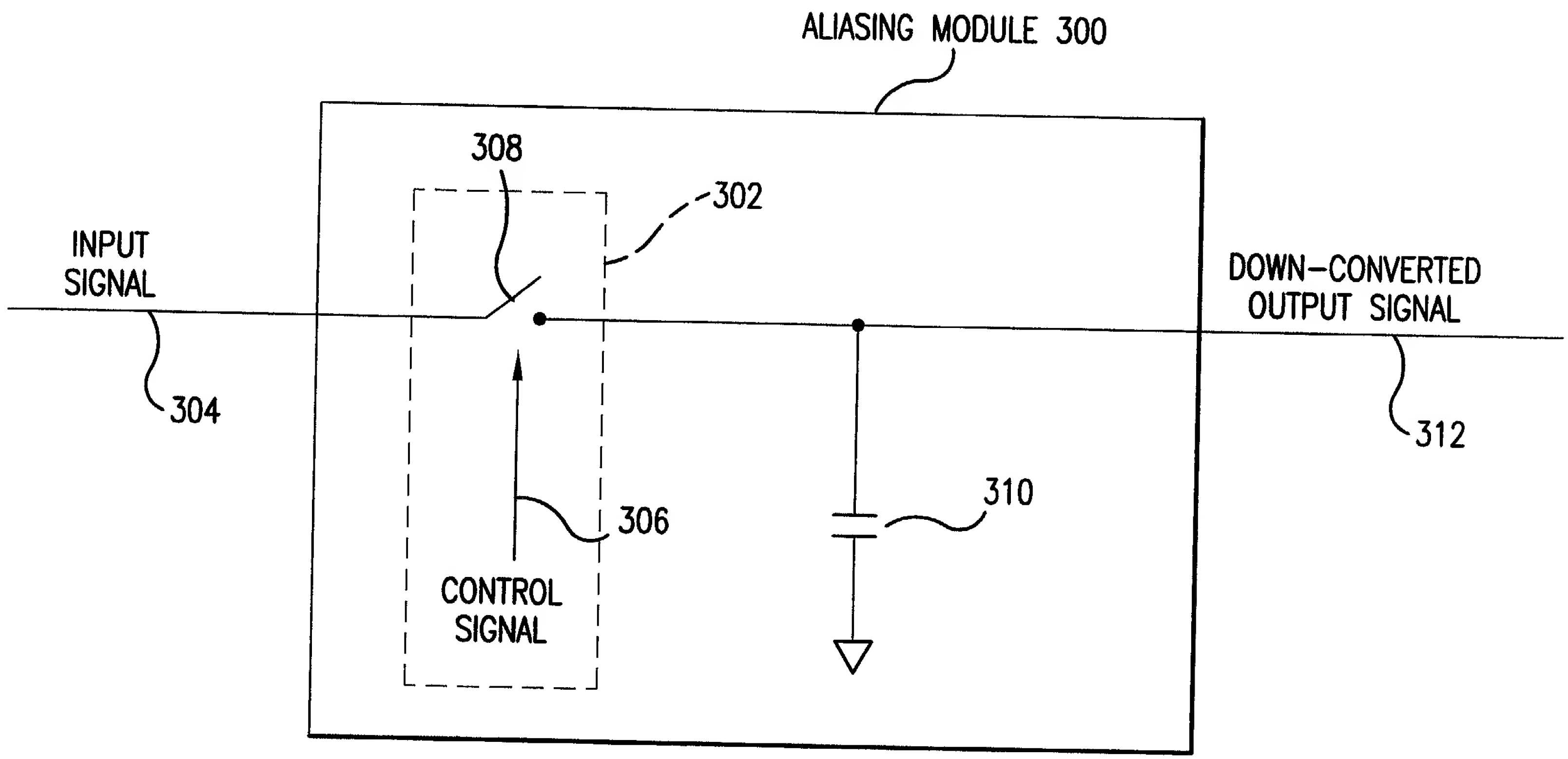
ALIASING MODULE 300
308
302
INPUT
SIGNAL
304
DOWN-CONVERTED
OUTPUT SIGNAL
312
306
CONTROL
SIGNAL
310

FIG. 3A

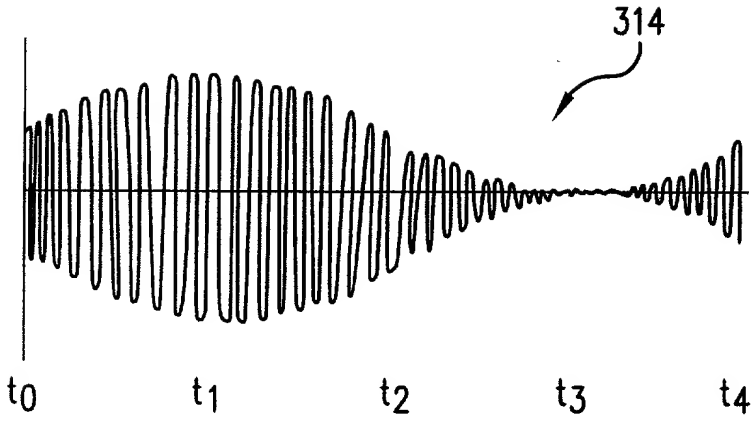

FIG. 3B

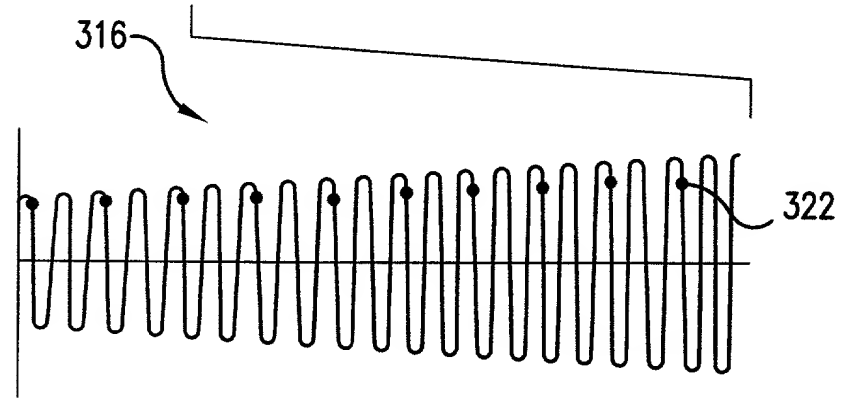

FIG. 3C

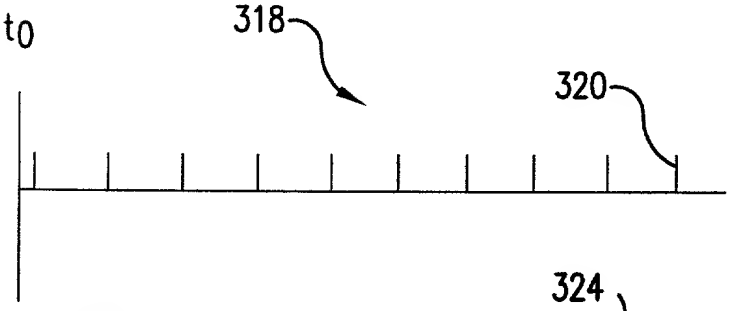

FIG. 3D

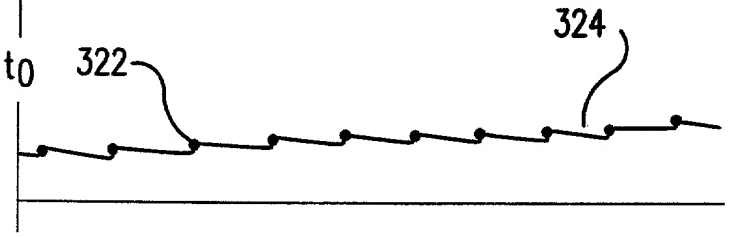

FIG. 3E

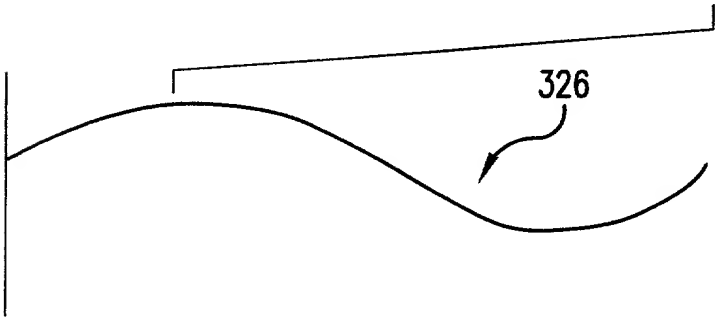

FIG. 3F

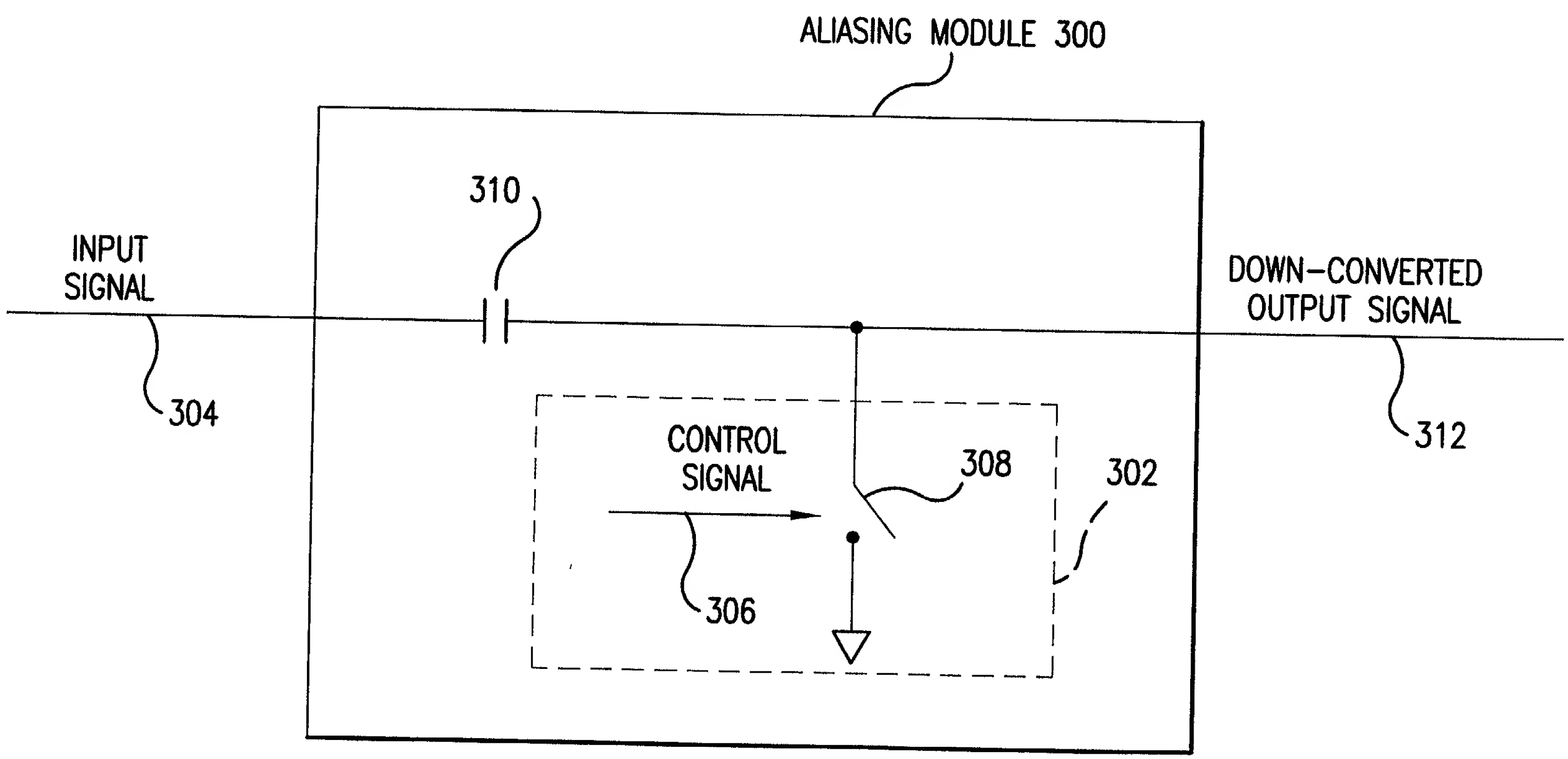
ALIASING MODULE 300
310
INPUT
SIGNAL
304
DOWN-CONVERTED
OUTPUT SIGNAL
312
CONTROL
SIGNAL
306
308
302

FIG. 3G

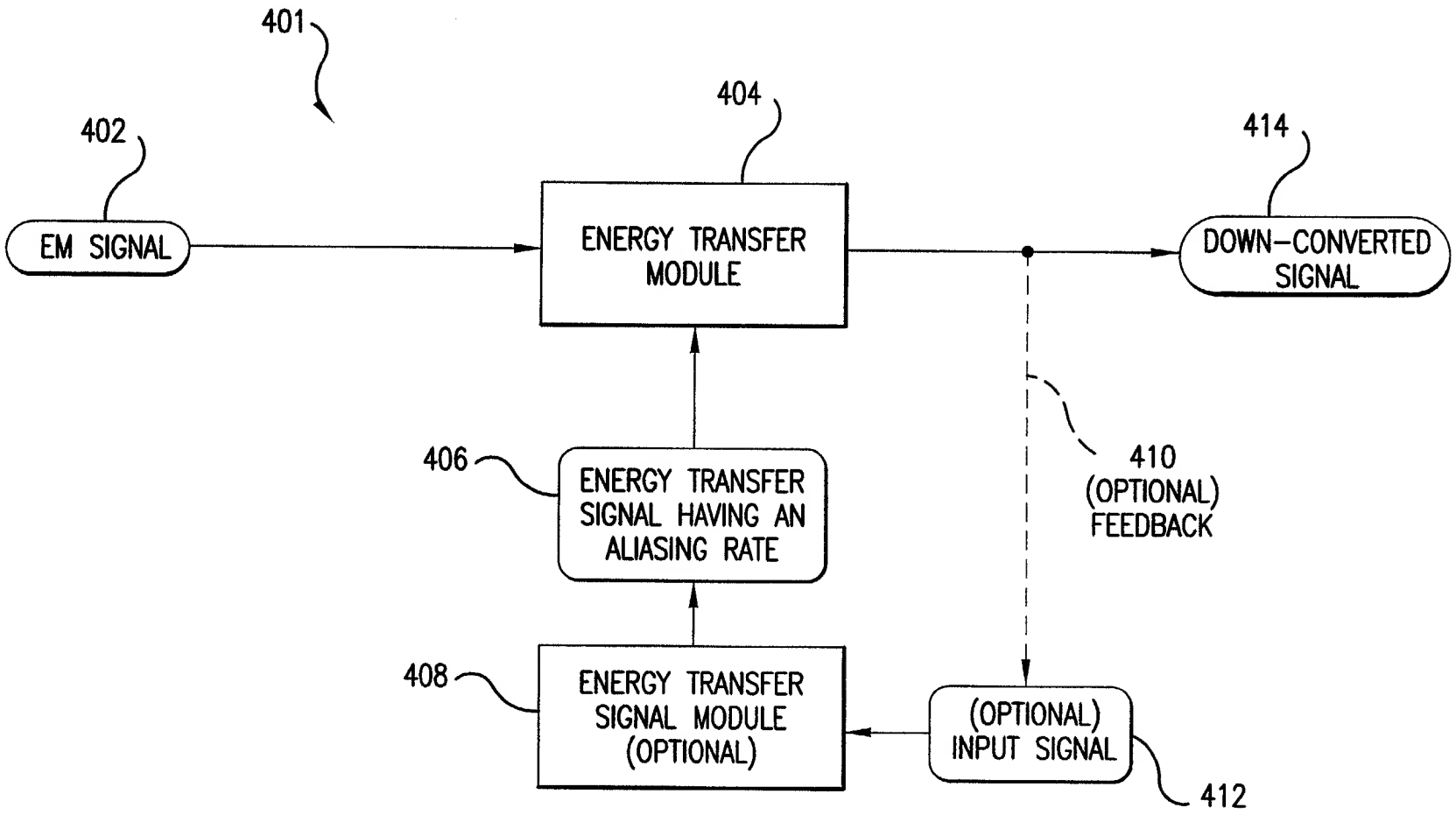

FIG. 4

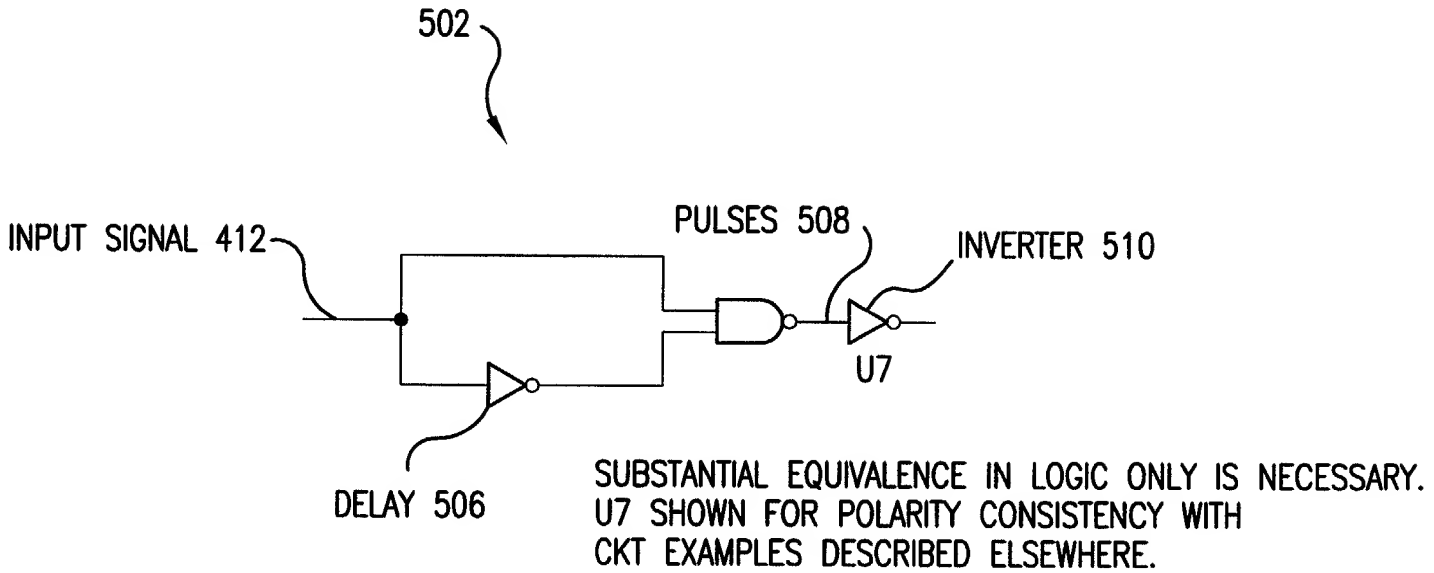

FIG. 5

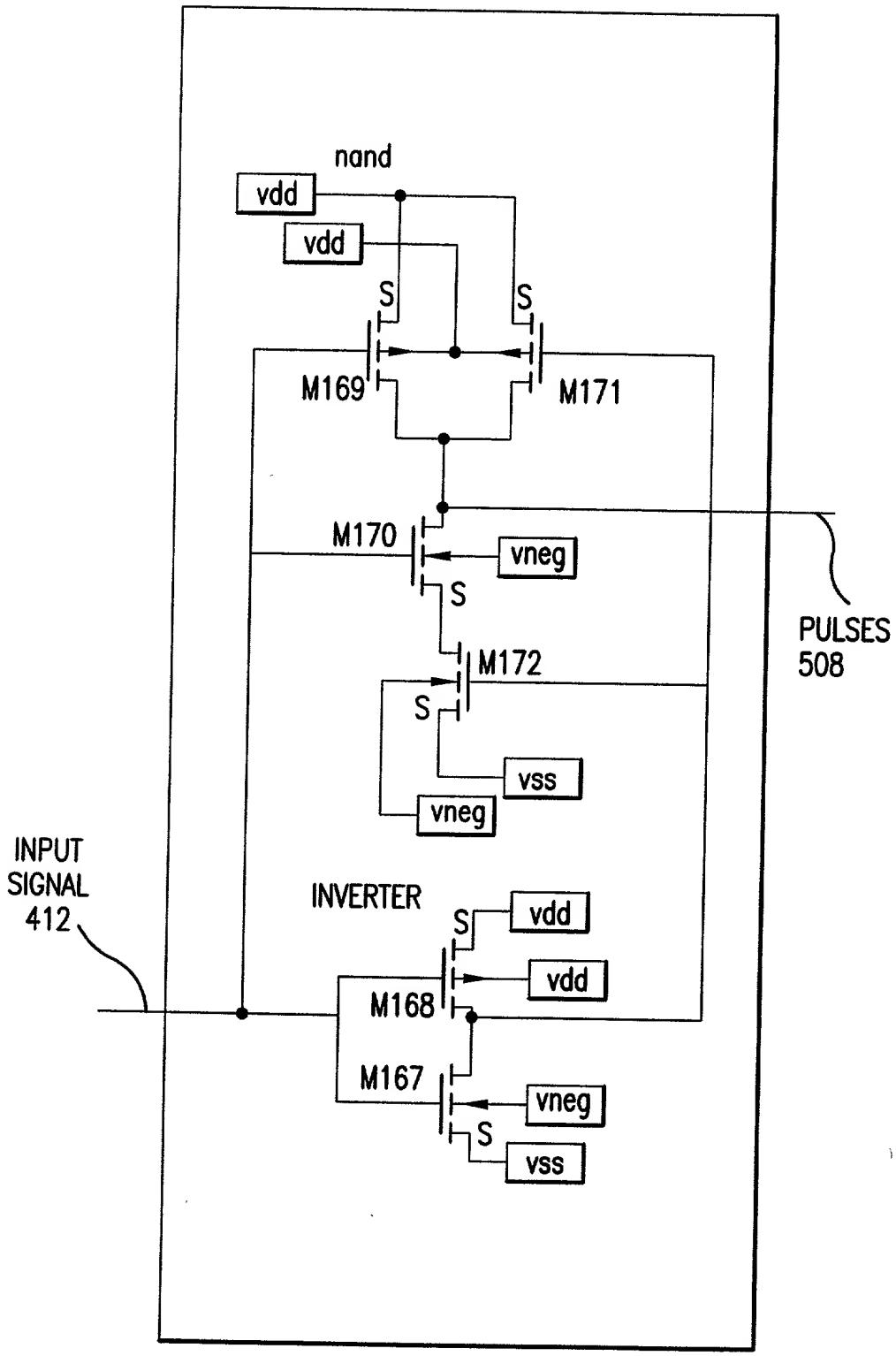
nand
vdd
vdd
S
S
M169
M171
M170
vneg
S
M172
S
vss
vneg
PULSES
508
INPUT
SIGNAL
412
INVERTER
S
vdd
vdd
M168
M167
vneg
S
vss

FIG. 6A

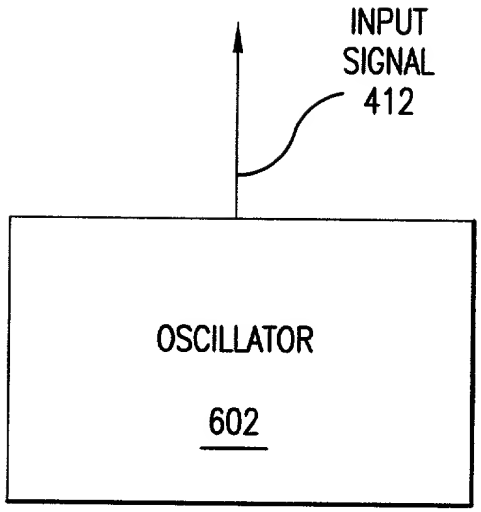

FIG. 6B

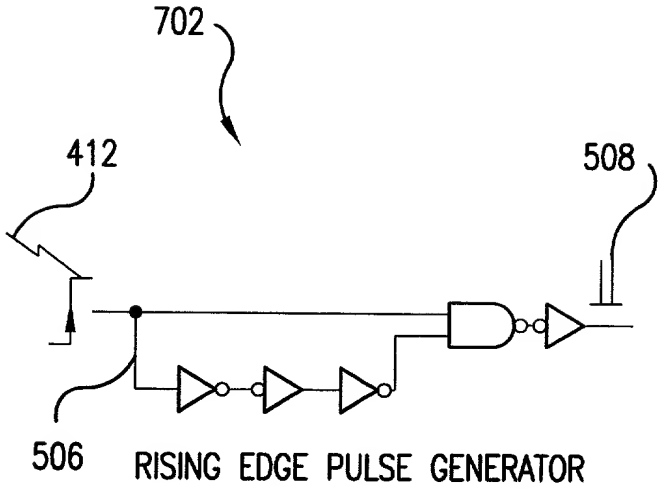
702
412
508
506
RISING EDGE PULSE GENERATOR

FIG. 7A

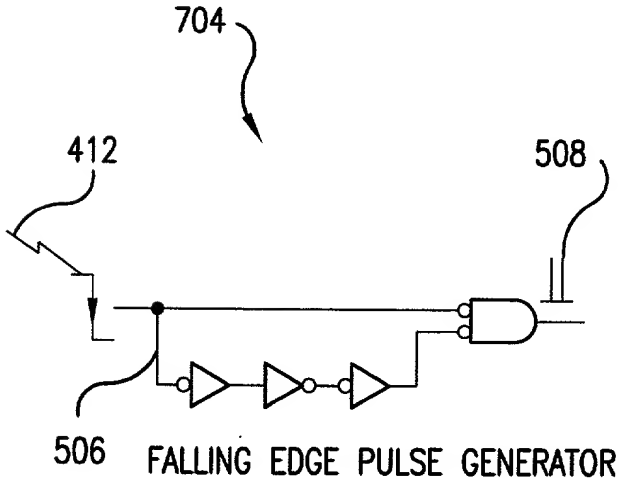
704
412
508
506
FALLING EDGE PULSE GENERATOR

FIG. 7B

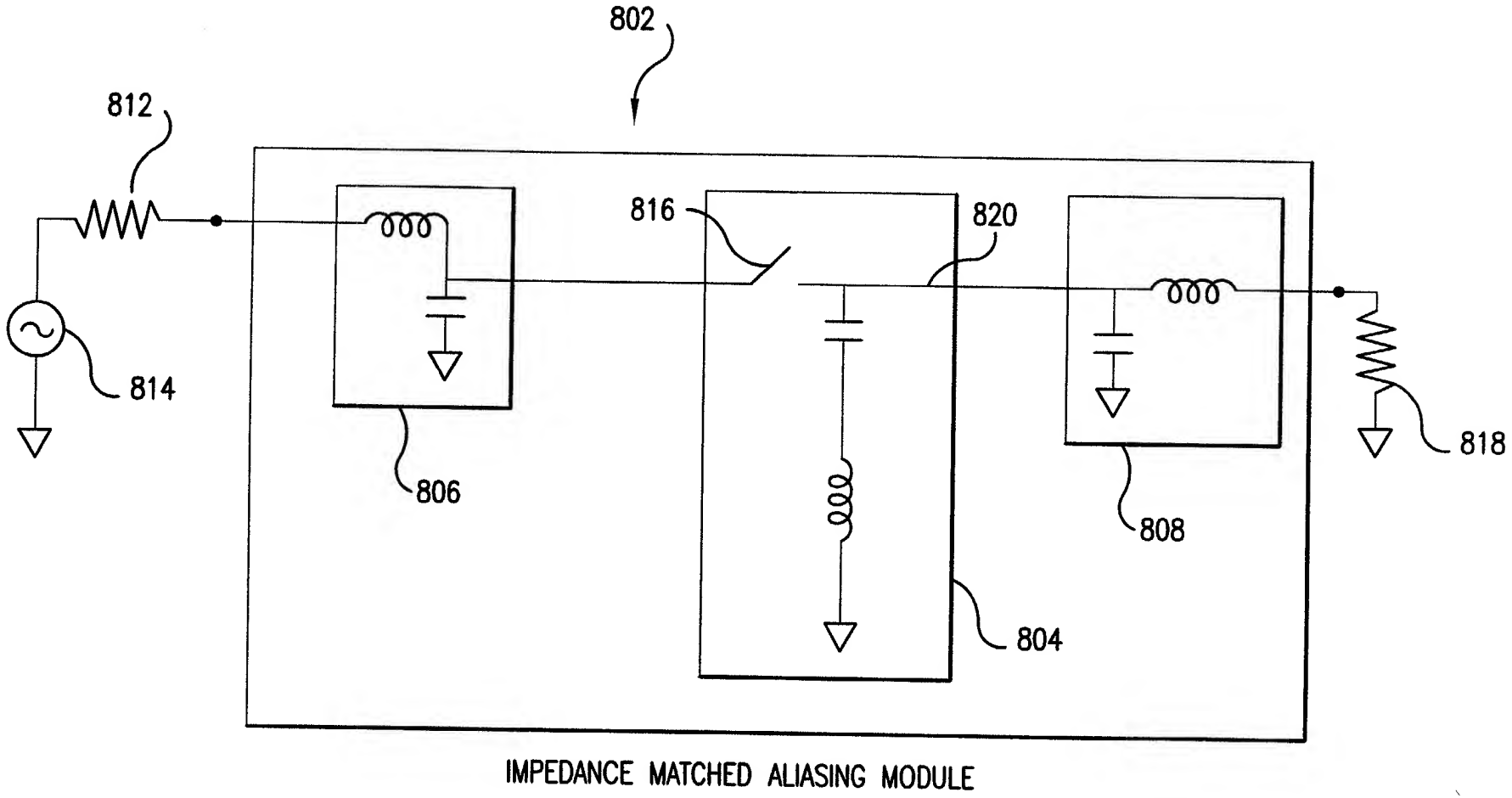

FIG. 8

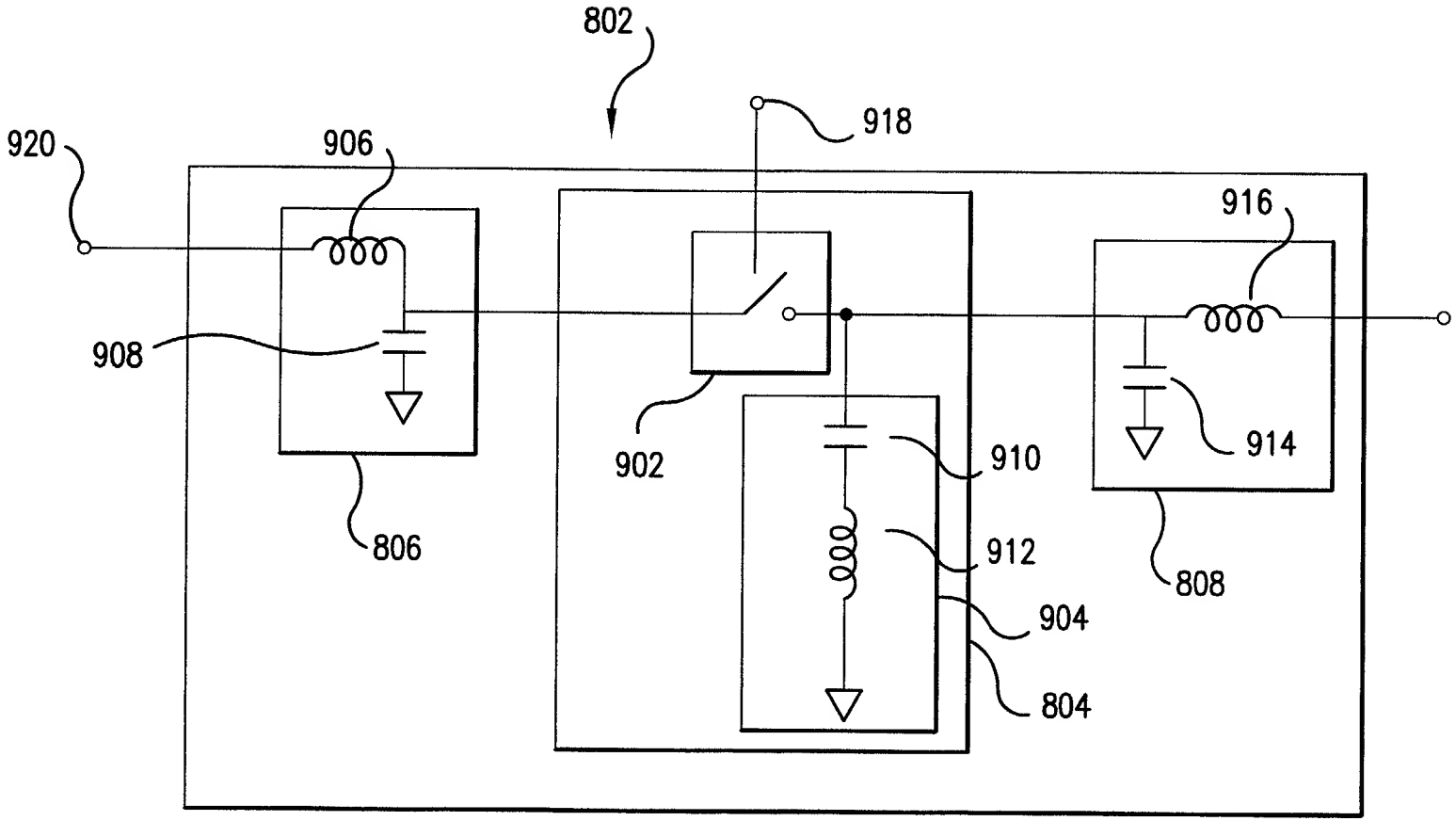

FIG. 9

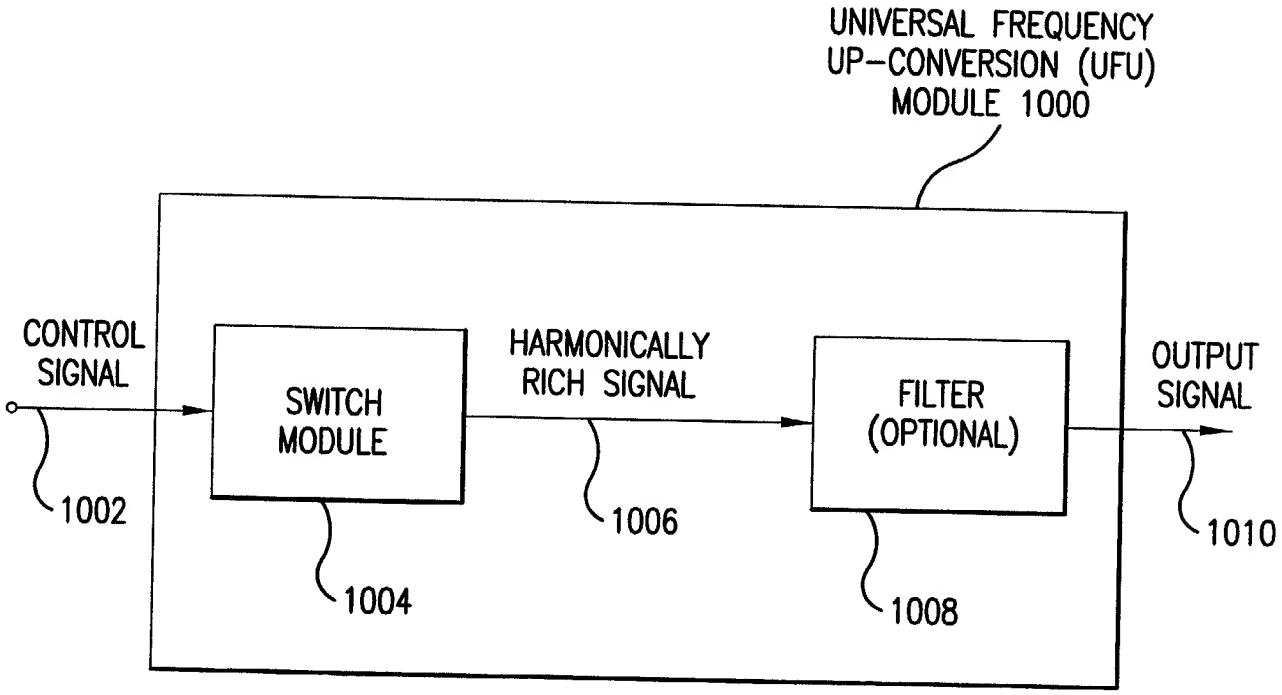

FIG. 10

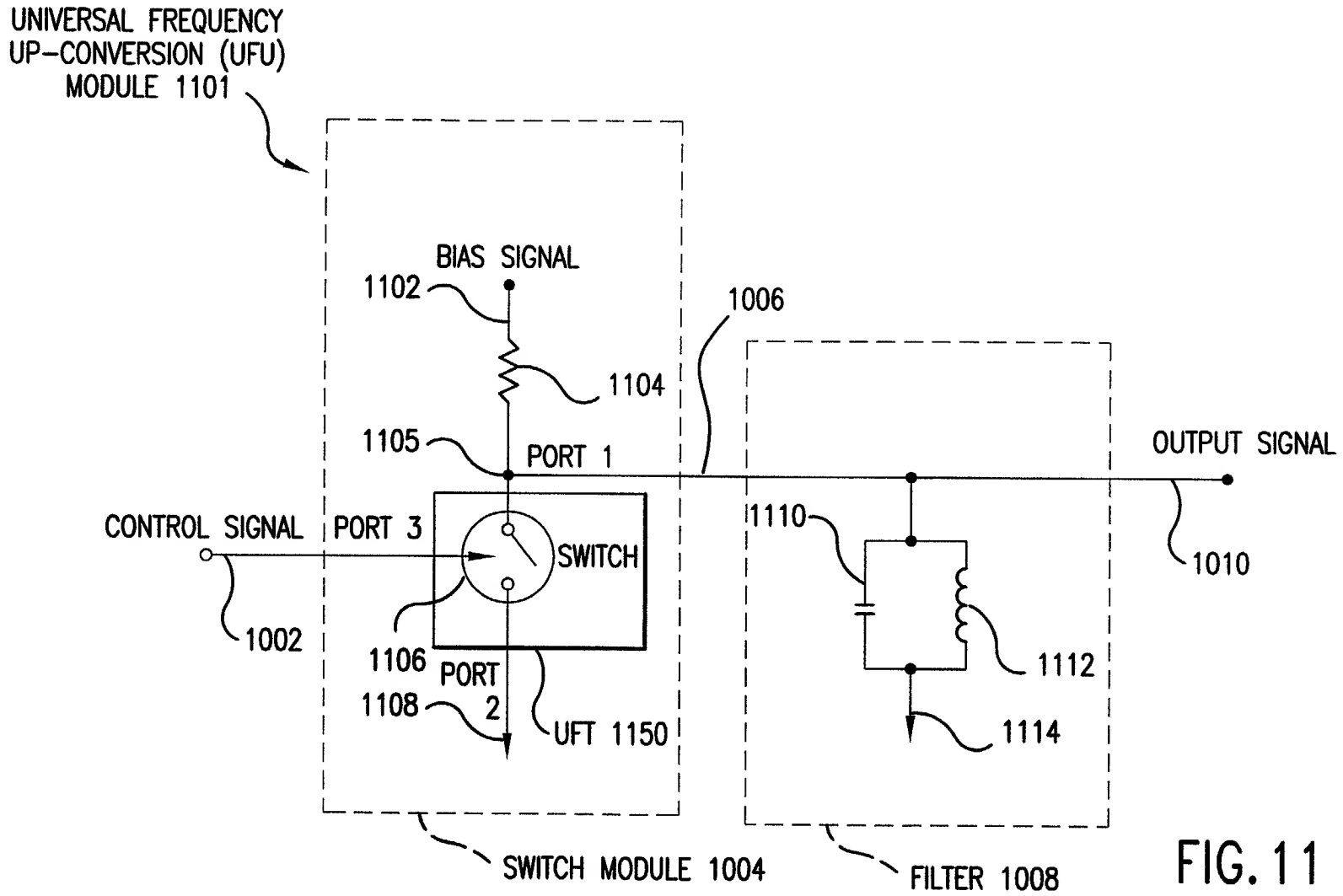

FIG. 11

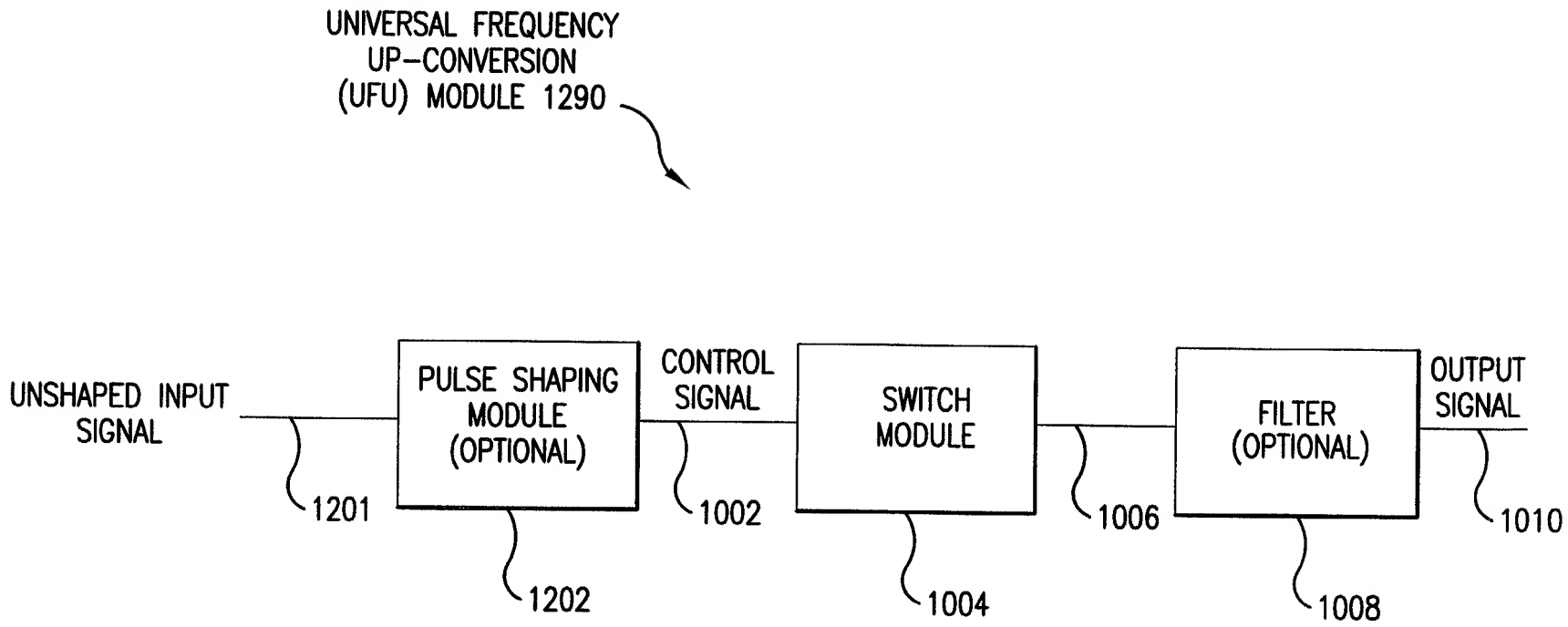

FIG. 12

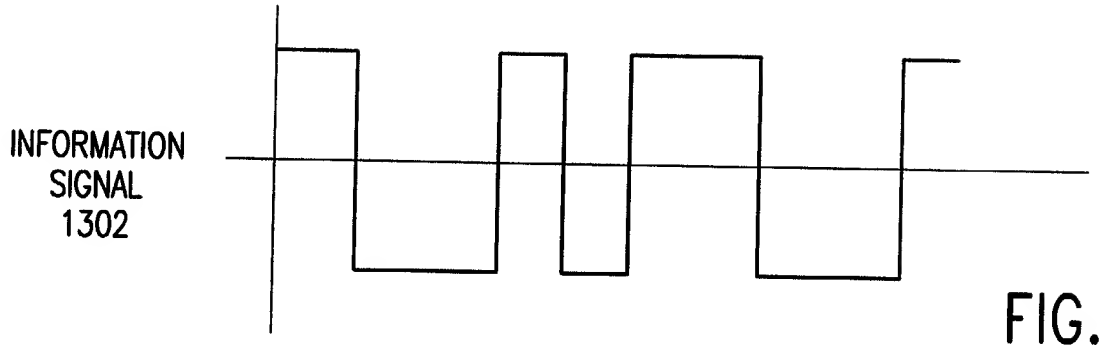

FIG. 13A

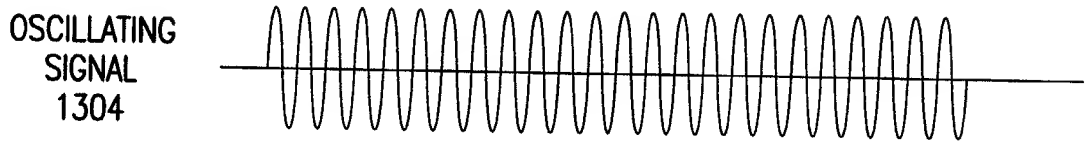

FIG. 13B

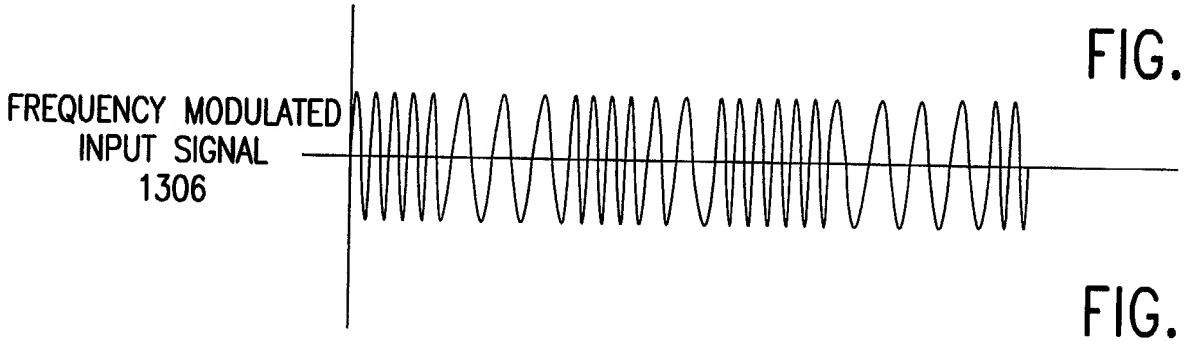

FIG. 13C

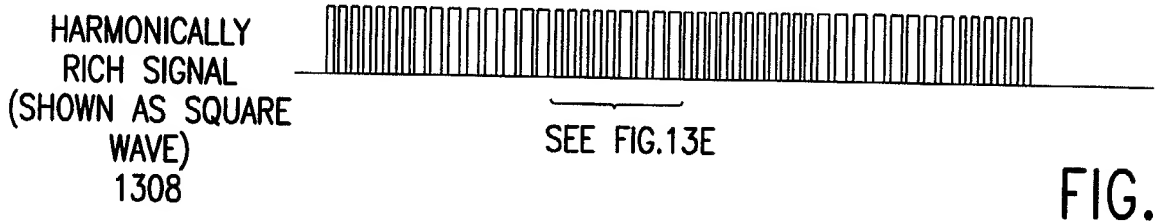

FIG. 13D

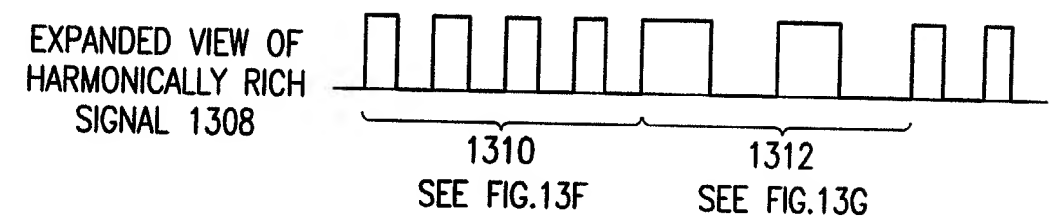

FIG. 13E

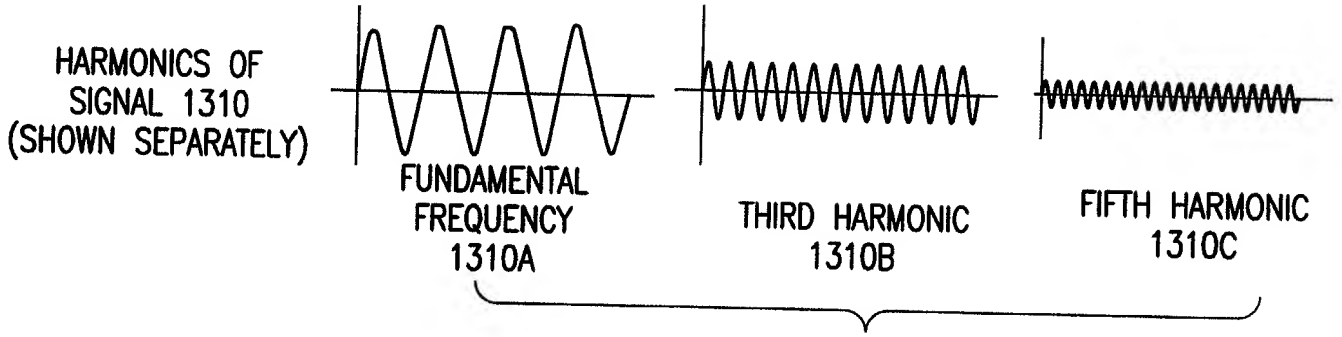

FIG. 13F

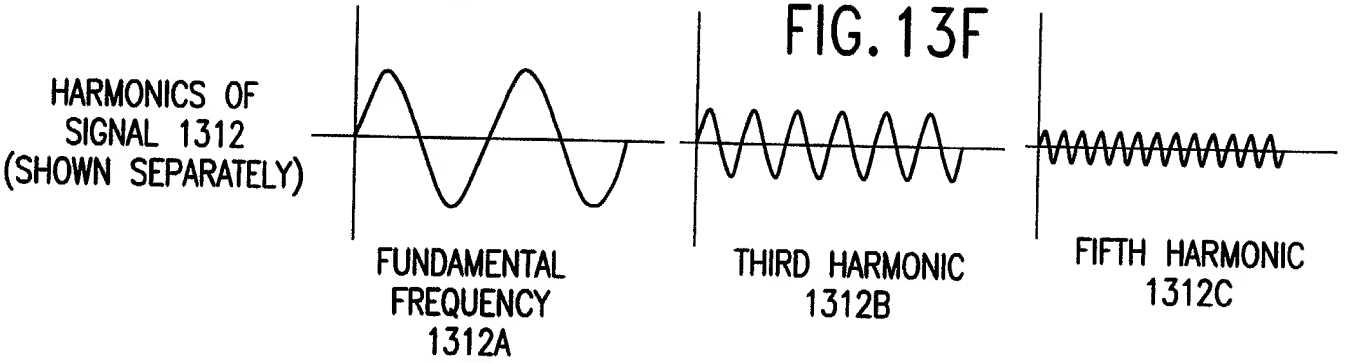

FIG. 13G

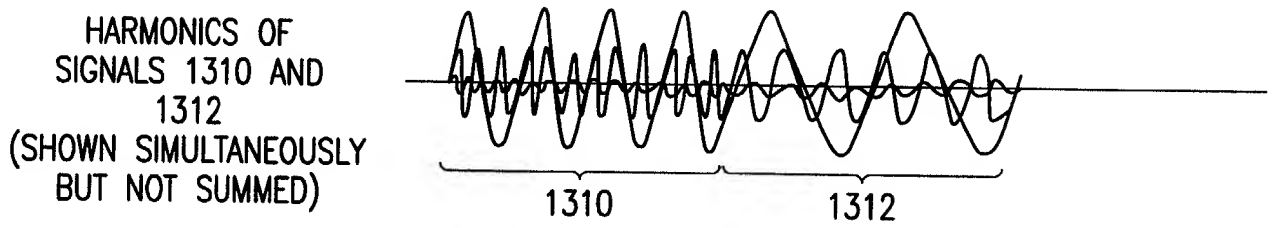

FIG. 13H

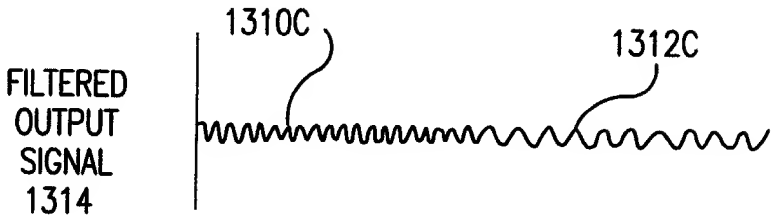

FIG. 13I

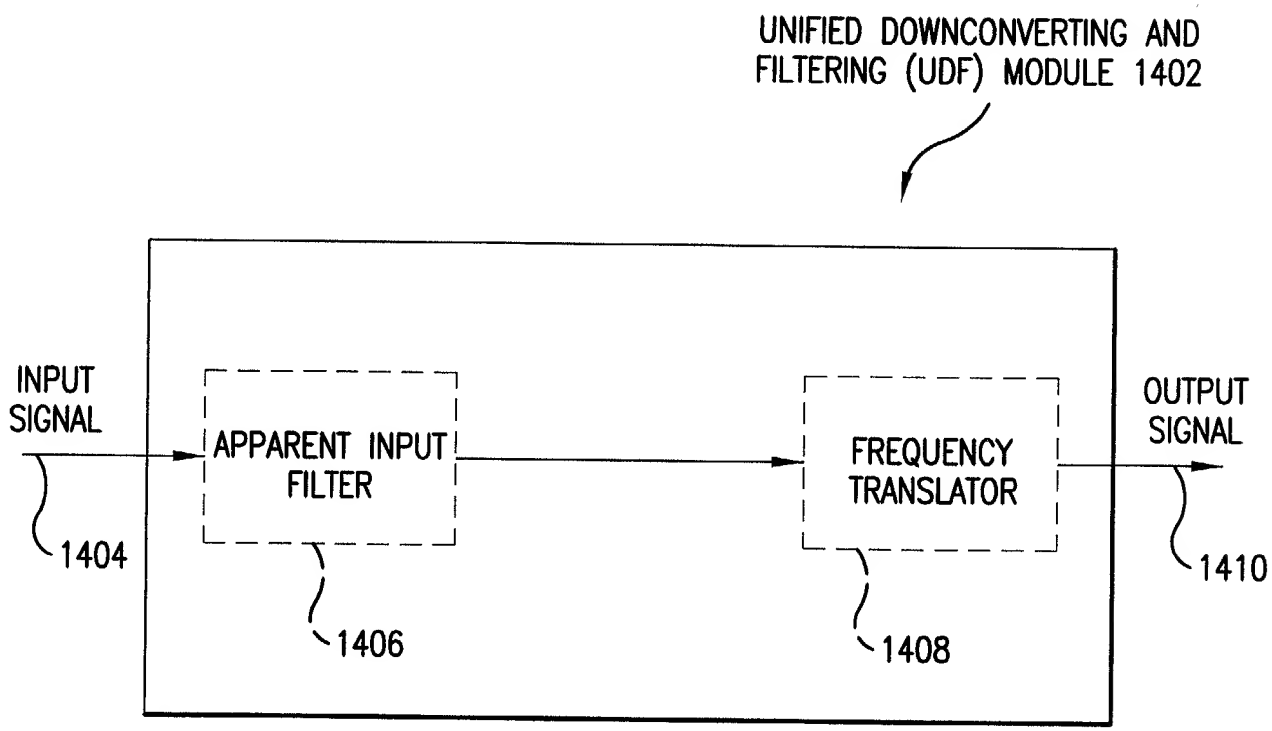

FIG. 14

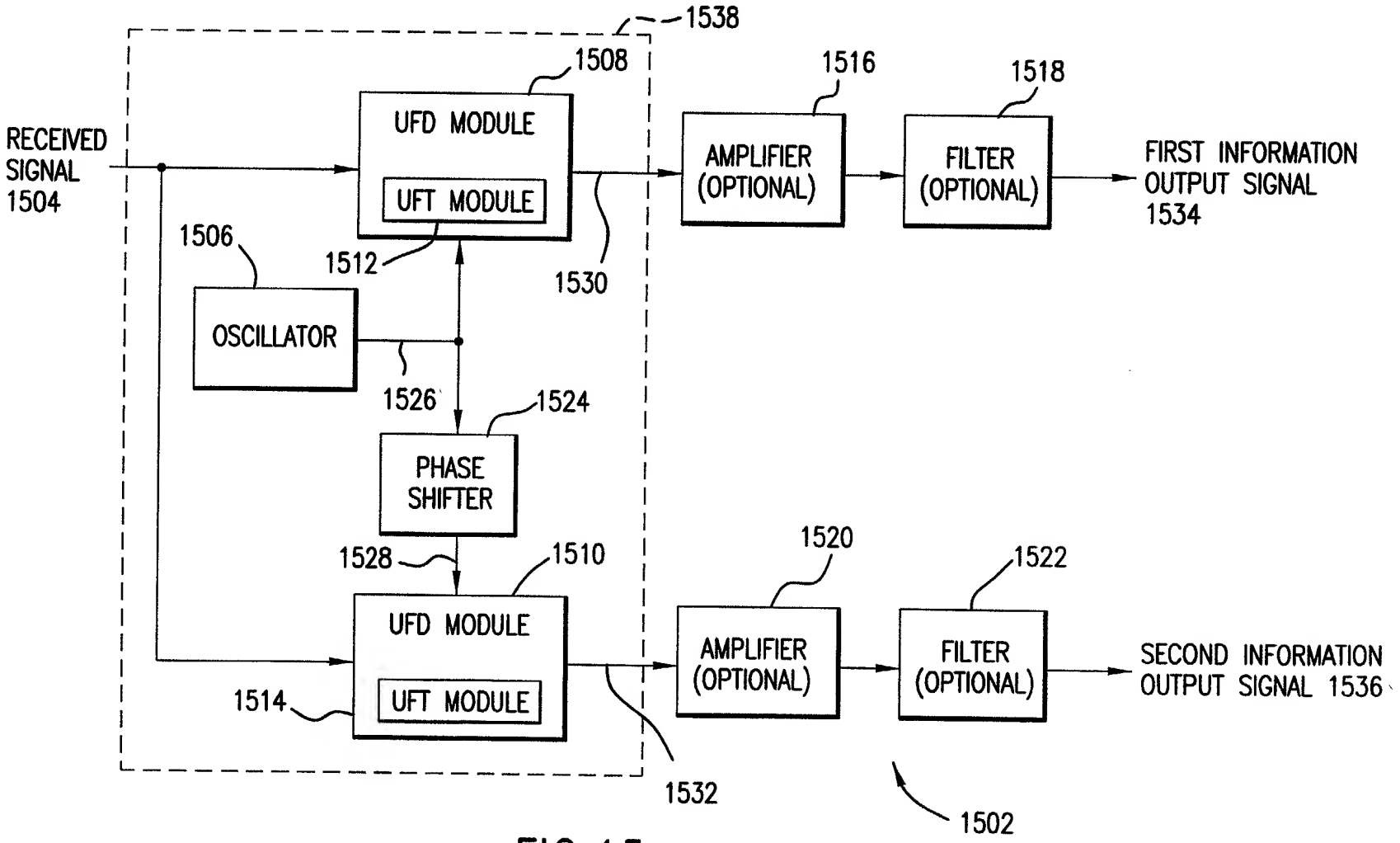

FIG.15

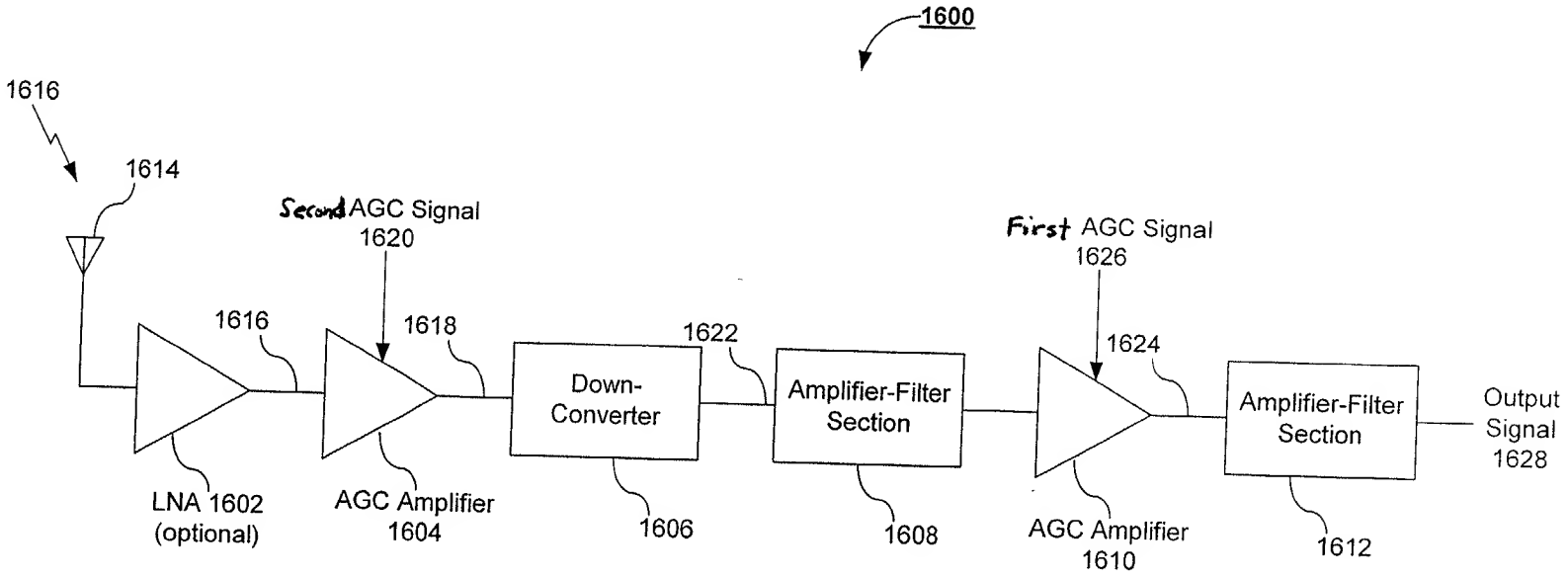

FIG. 16

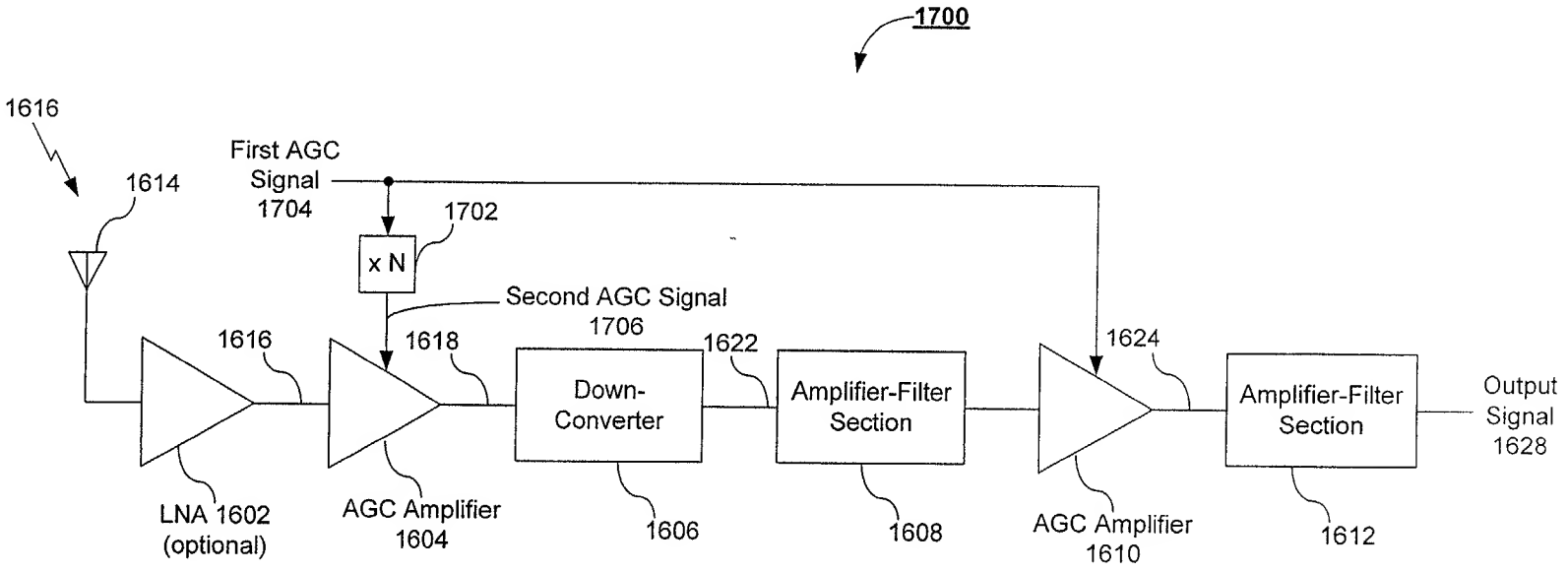

FIG. 17

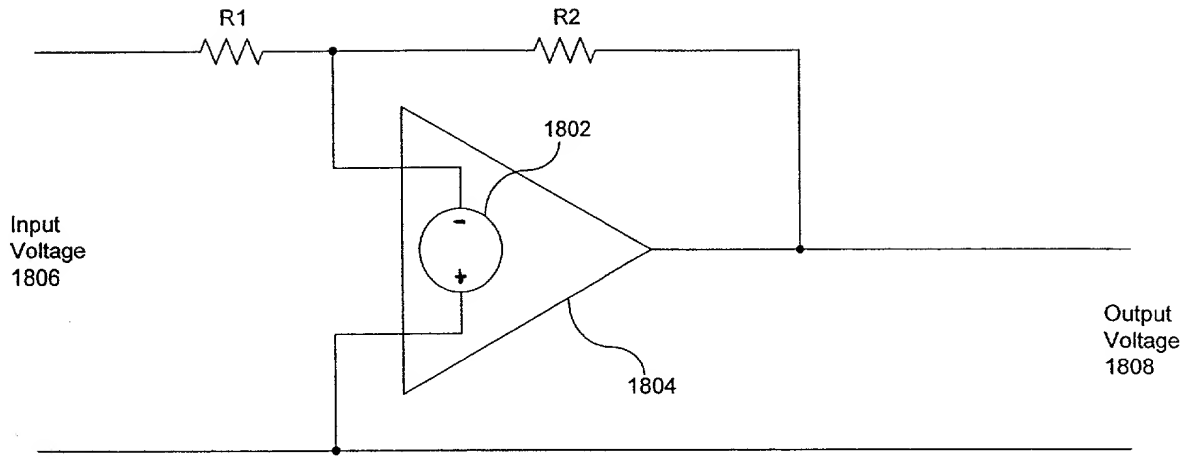
R1
R2
1802
Input
Voltage
1806
Output
Voltage
1808
1804

FIG. 18

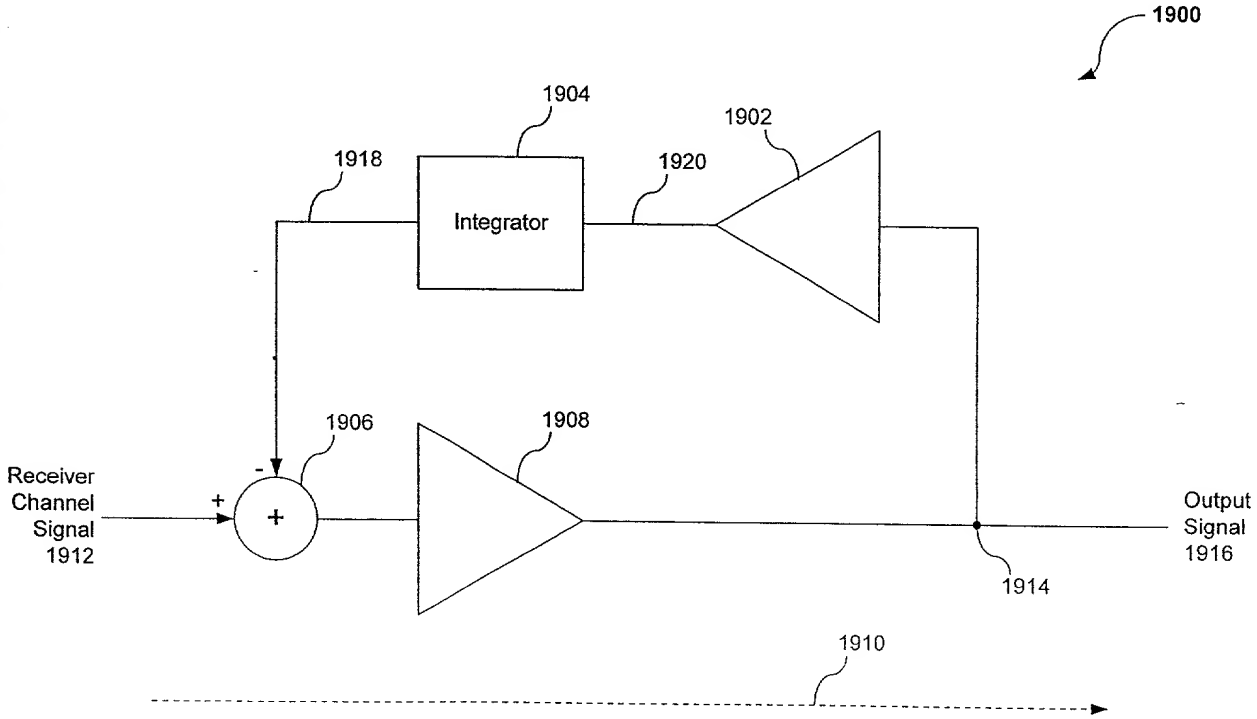
1900
1904
1902
1918
1920
Integrator
1906
1908
Receiver
Channel
Signal
1912
Output
Signal
1916
1914
1910

FIG. 19

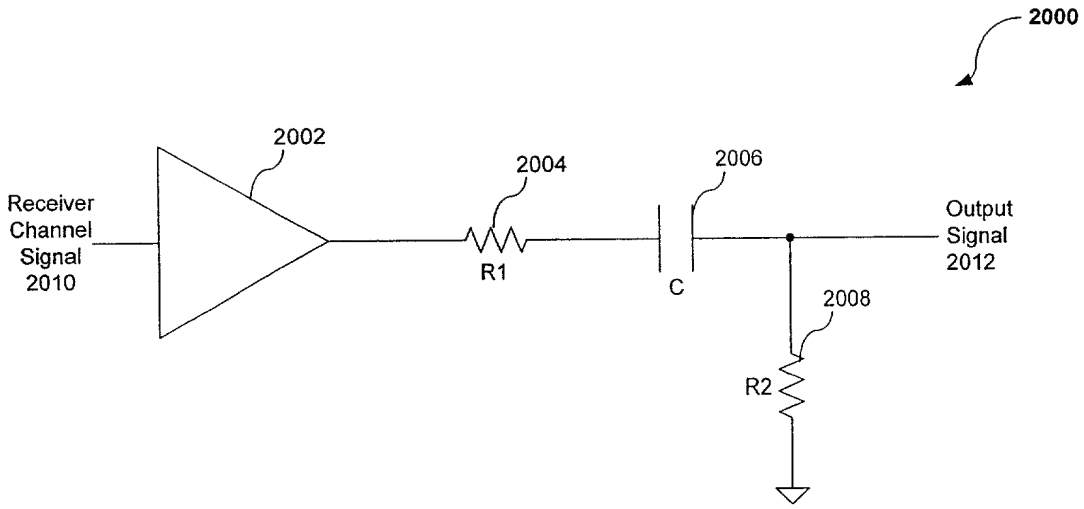
2000
2002
2004
2006
Receiver
Channel
Signal
2010
R1
C
Output
Signal
2012
2008
R2

FIG. 20

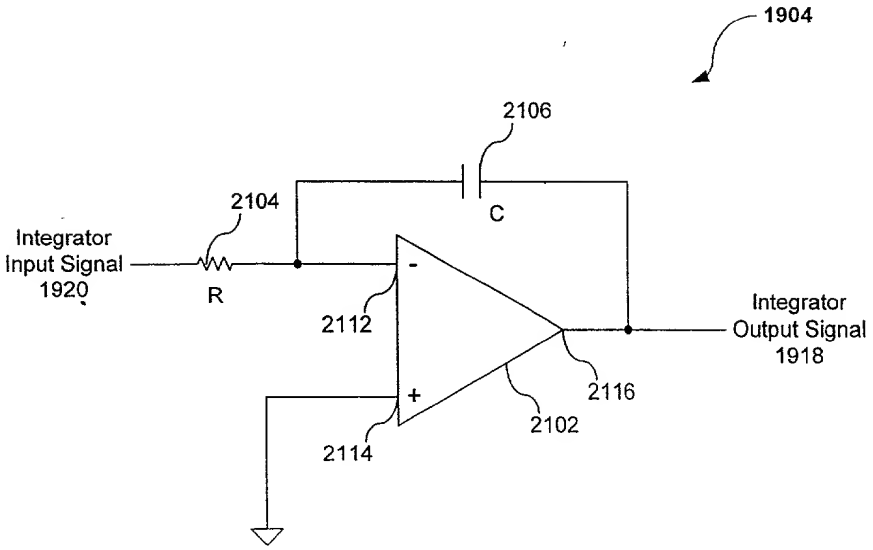
1904
2106
C
2104
Integrator
Input Signal
1920
R
2112
-
+
Integrator
Output Signal
1918
2116
2102
2114

FIG. 21

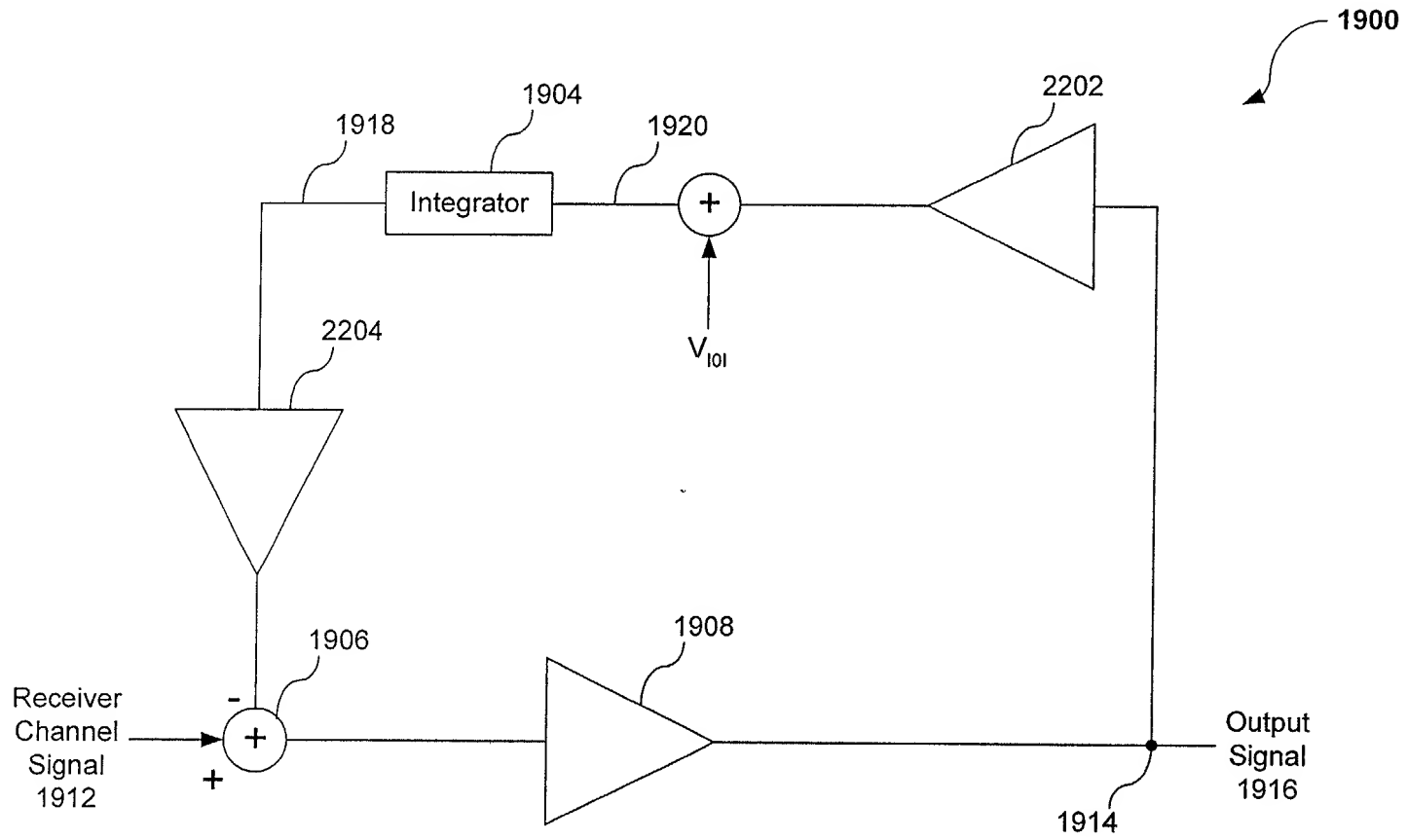

FIG. 22

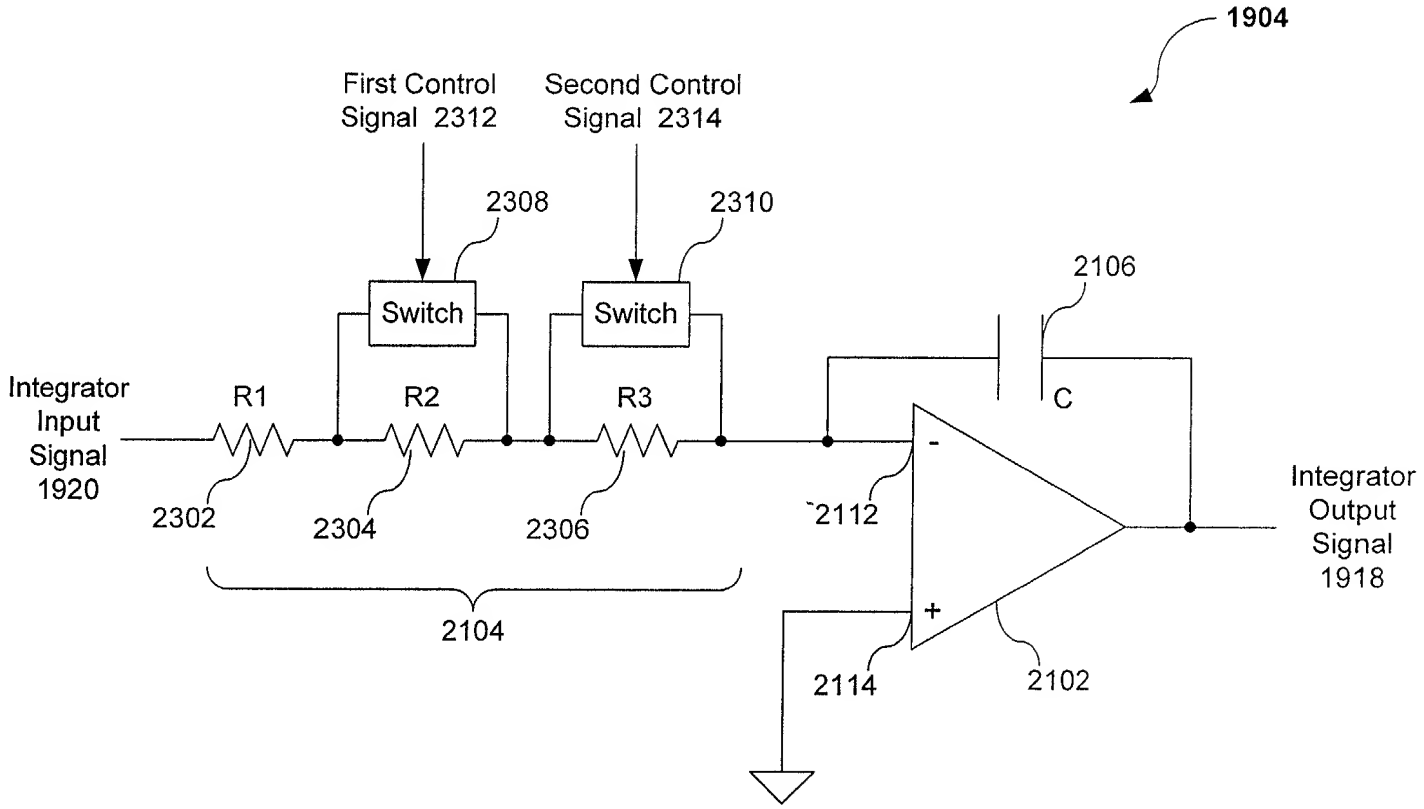

FIG. 23

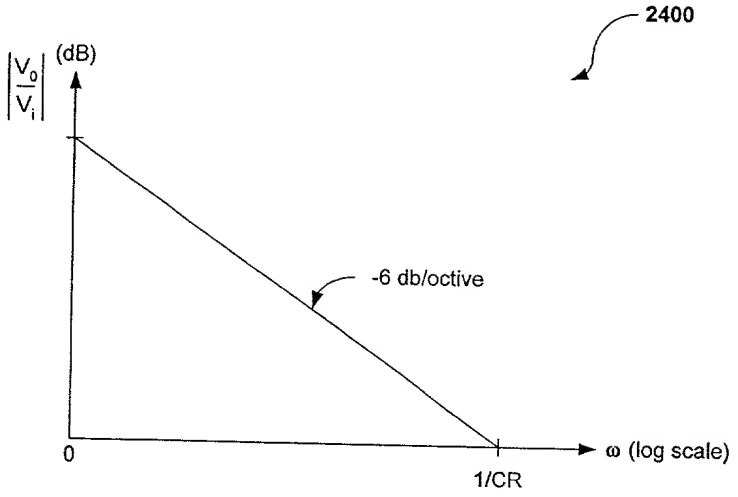

FIG. 24A

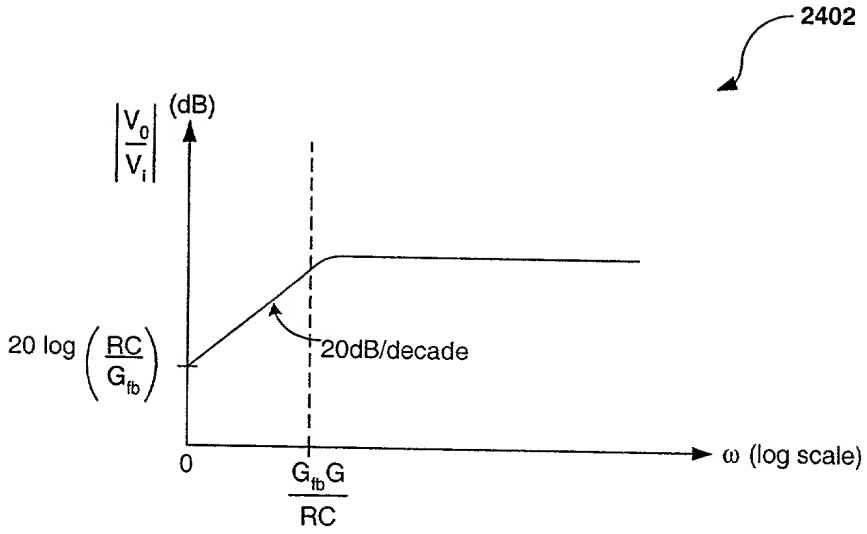

FIG. 24B

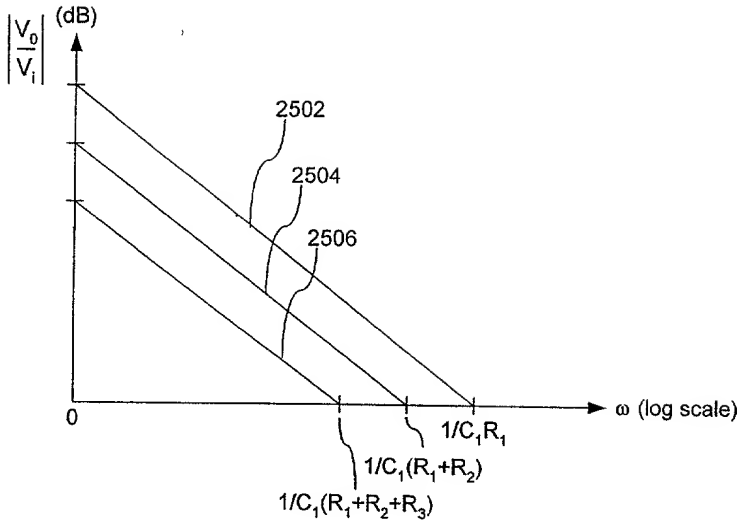

FIG. 25A

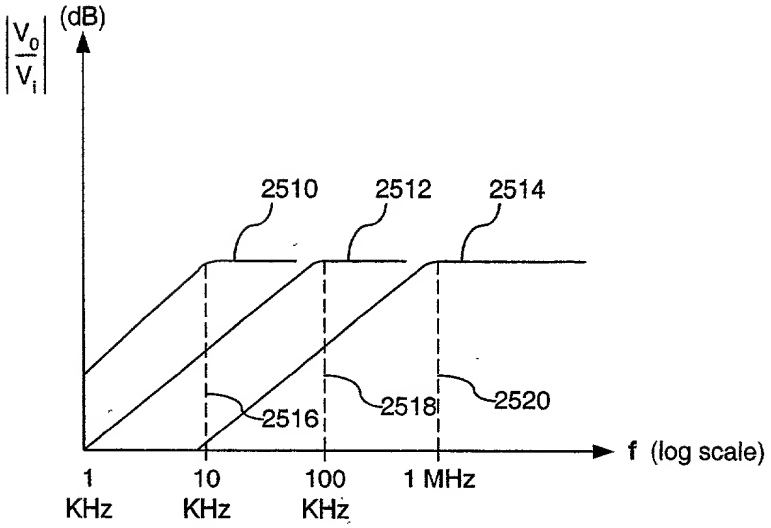

FIG. 25B

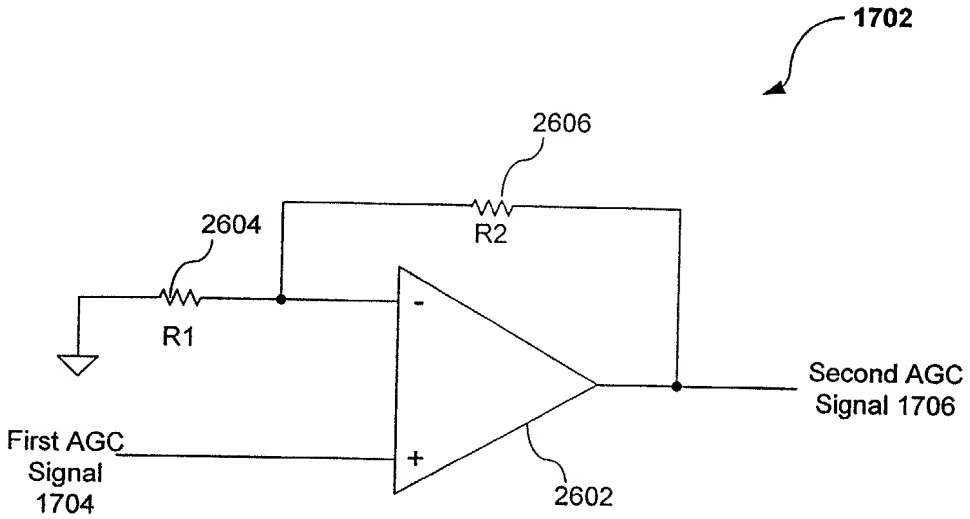

FIG. 26

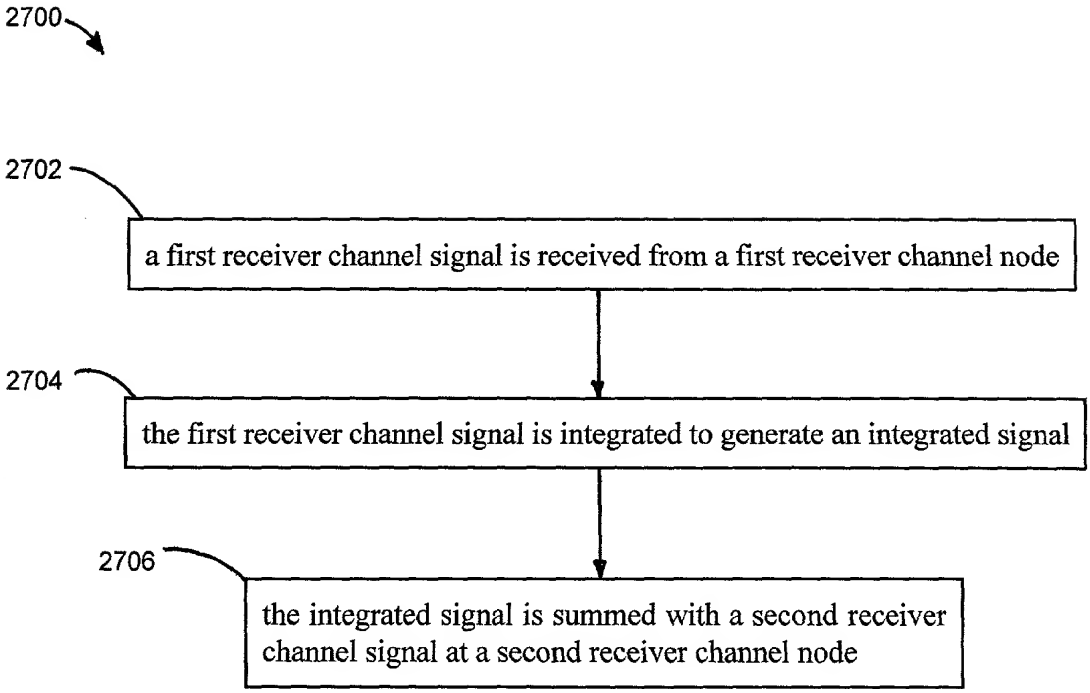
2700
2702
a first receiver channel signal is received from a first receiver channel node
2704
the first receiver channel signal is integrated to generate an integrated signal
2706
the integrated signal is summed with a second receiver channel signal at a second receiver channel node

FIG. 27

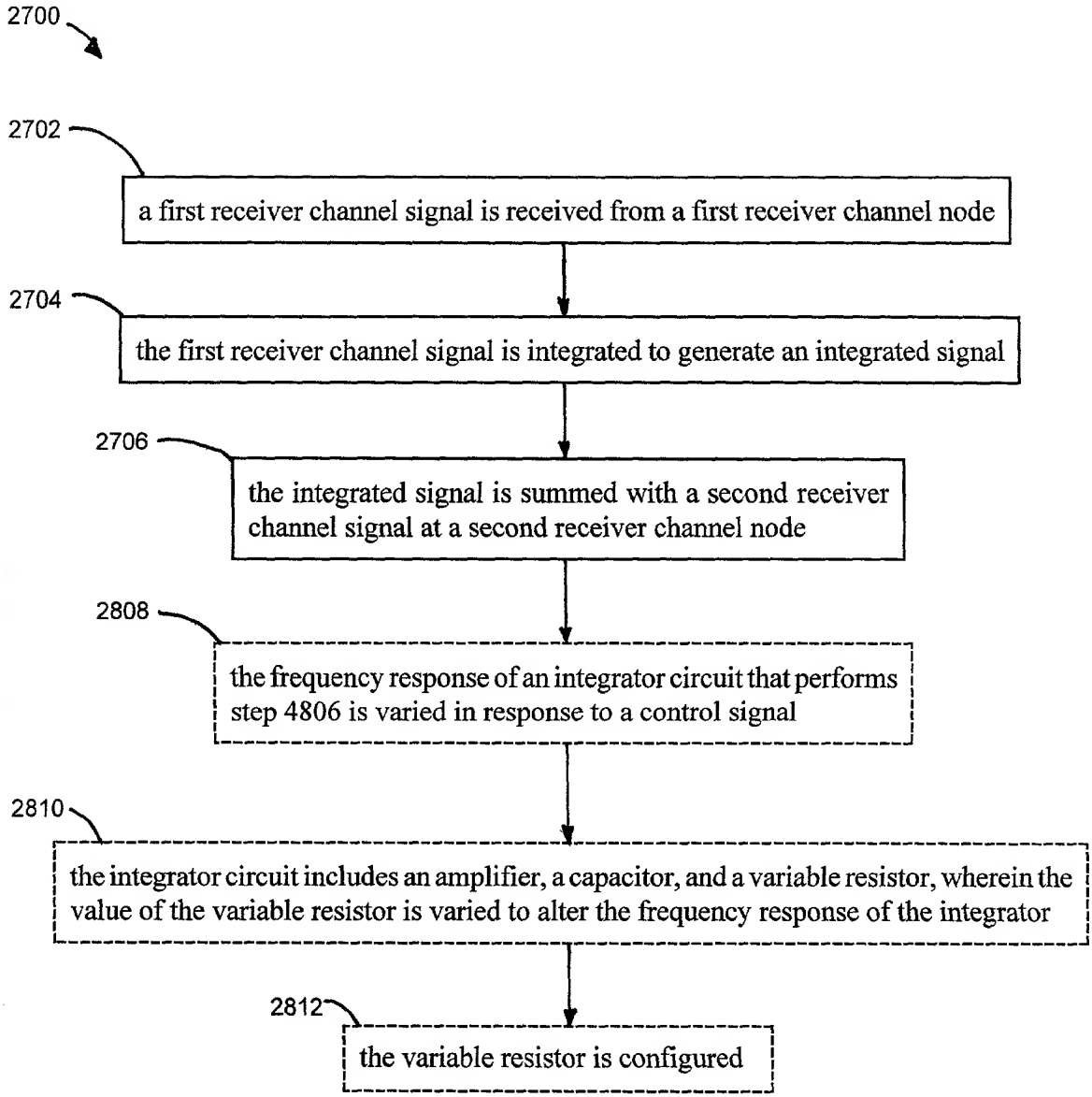
2700
2702
a first receiver channel signal is received from a first receiver channel node
2704
the first receiver channel signal is integrated to generate an integrated signal
2706
the integrated signal is summed with a second receiver channel signal at a second receiver channel node
2808
the frequency response of an integrator circuit that performs step 4806 is varied in response to a control signal
2810
the integrator circuit includes an amplifier, a capacitor, and a variable resistor, wherein the value of the variable resistor is varied to alter the frequency response of the integrator
2812
the variable resistor is configured

FIG. 28

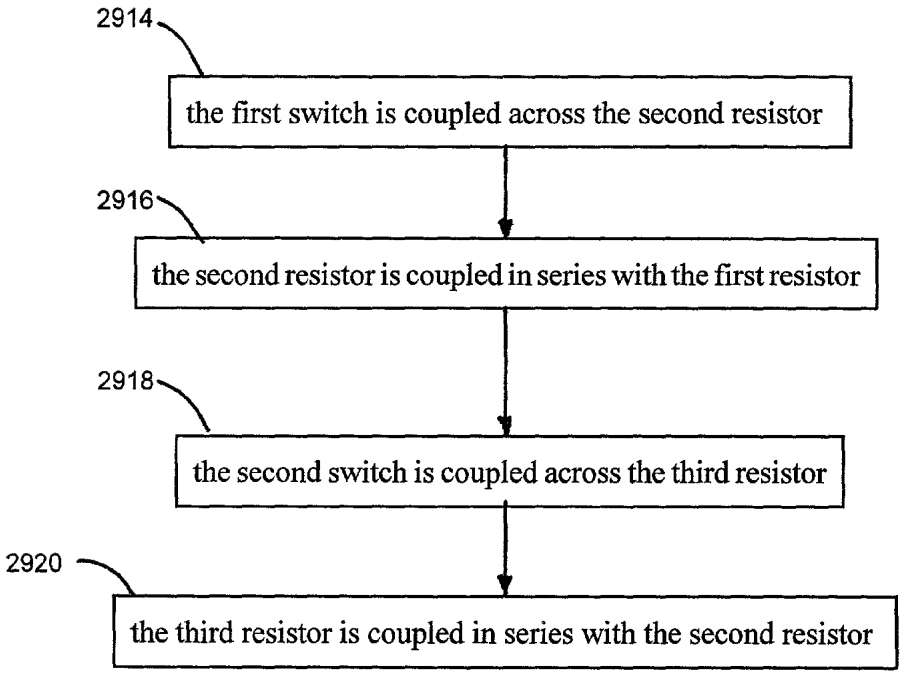
2914
the first switch is coupled across the second resistor
2916
the second resistor is coupled in series with the first resistor
2918
the second switch is coupled across the third resistor
2920
the third resistor is coupled in series with the second resistor

FIG. 29

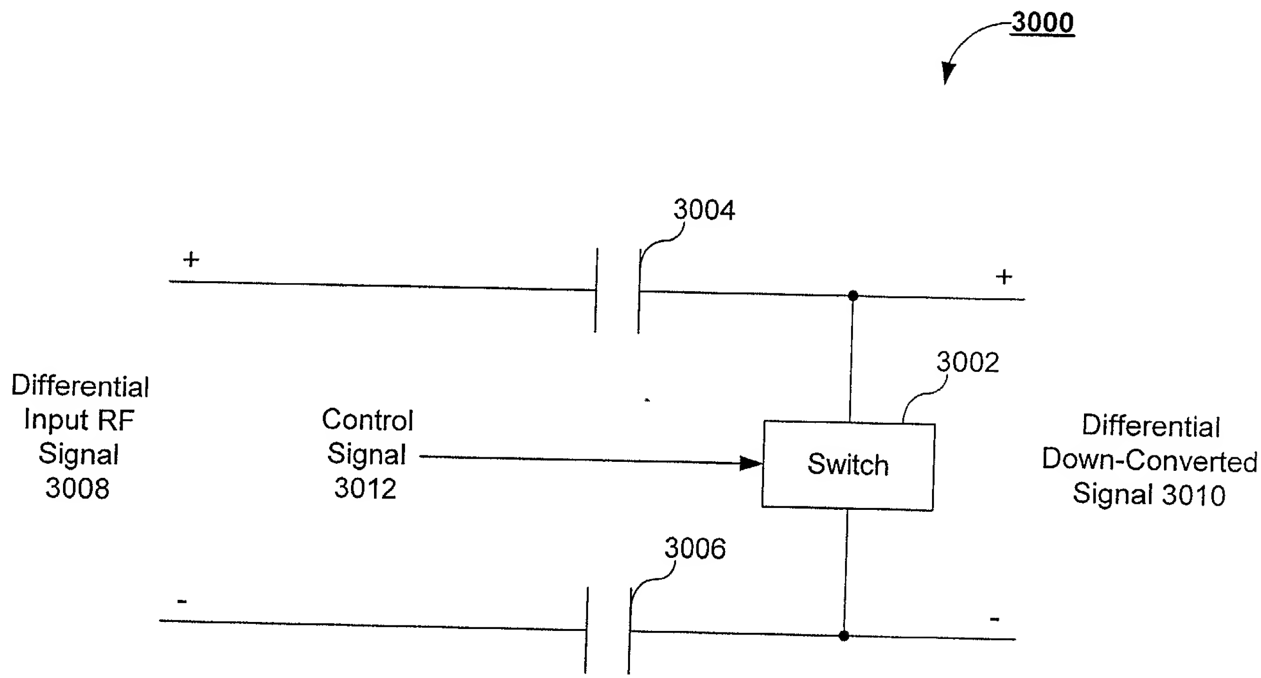

FIG. 30

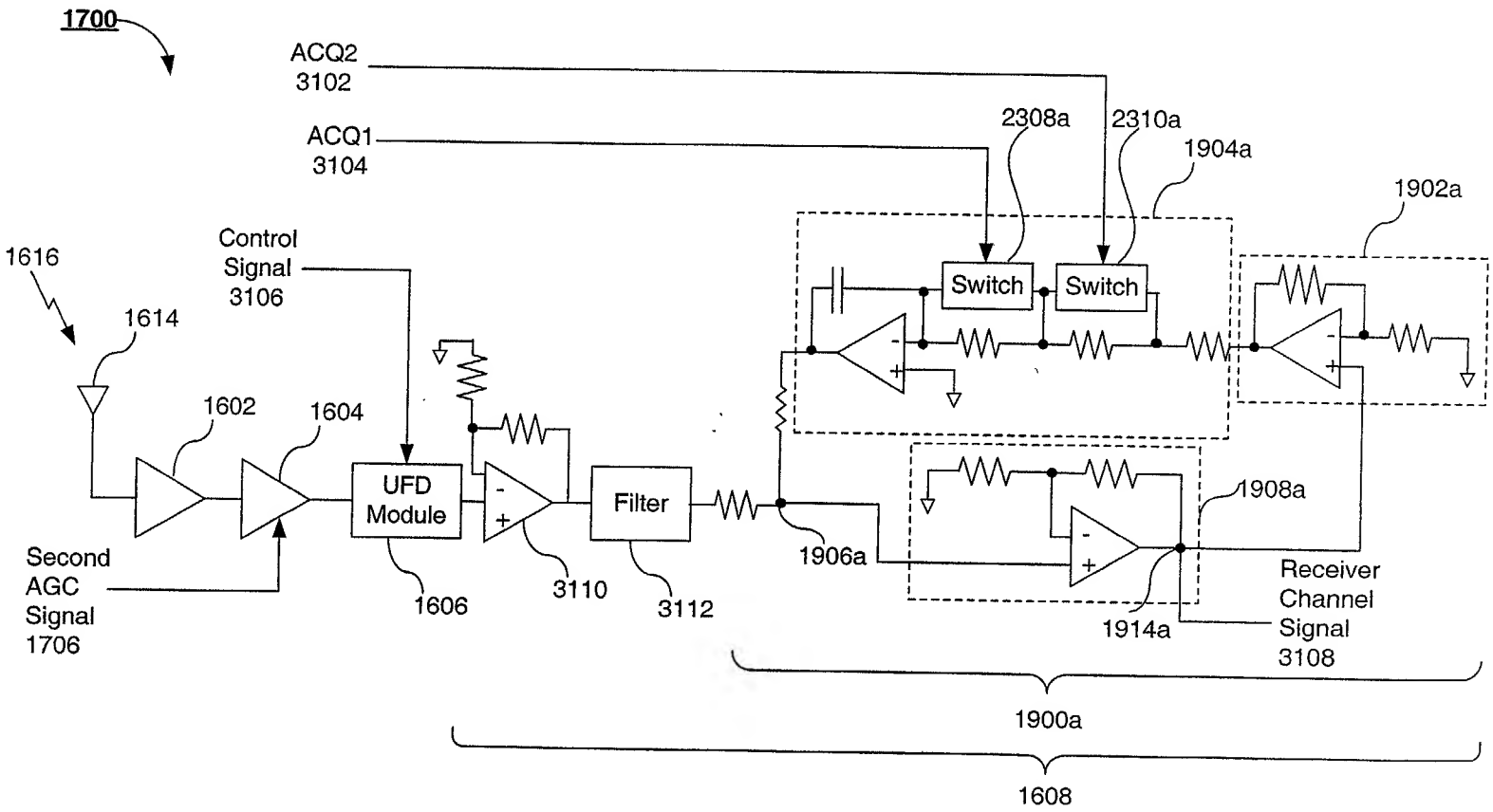

FIG. 31A

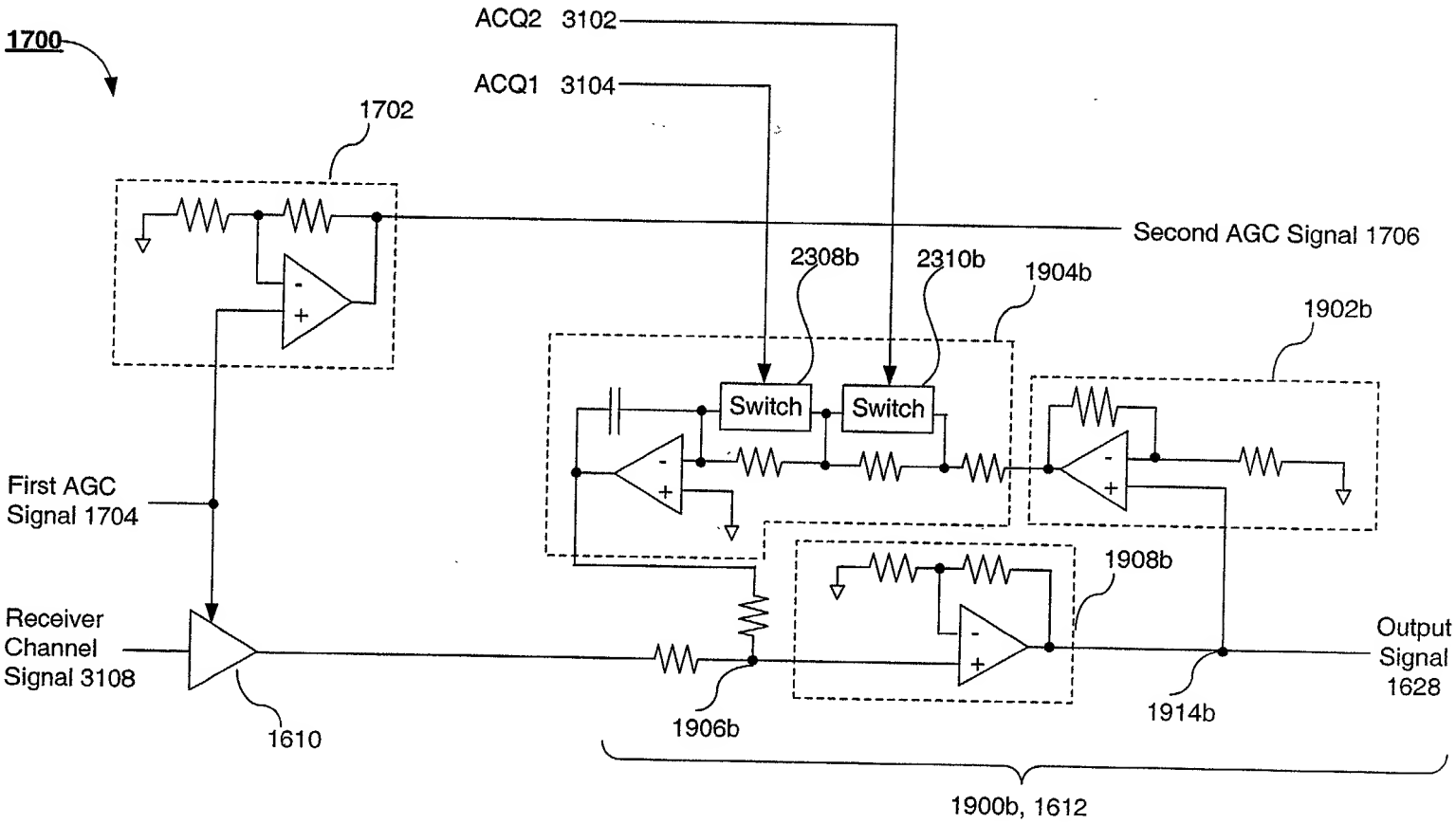

FIG. 31B

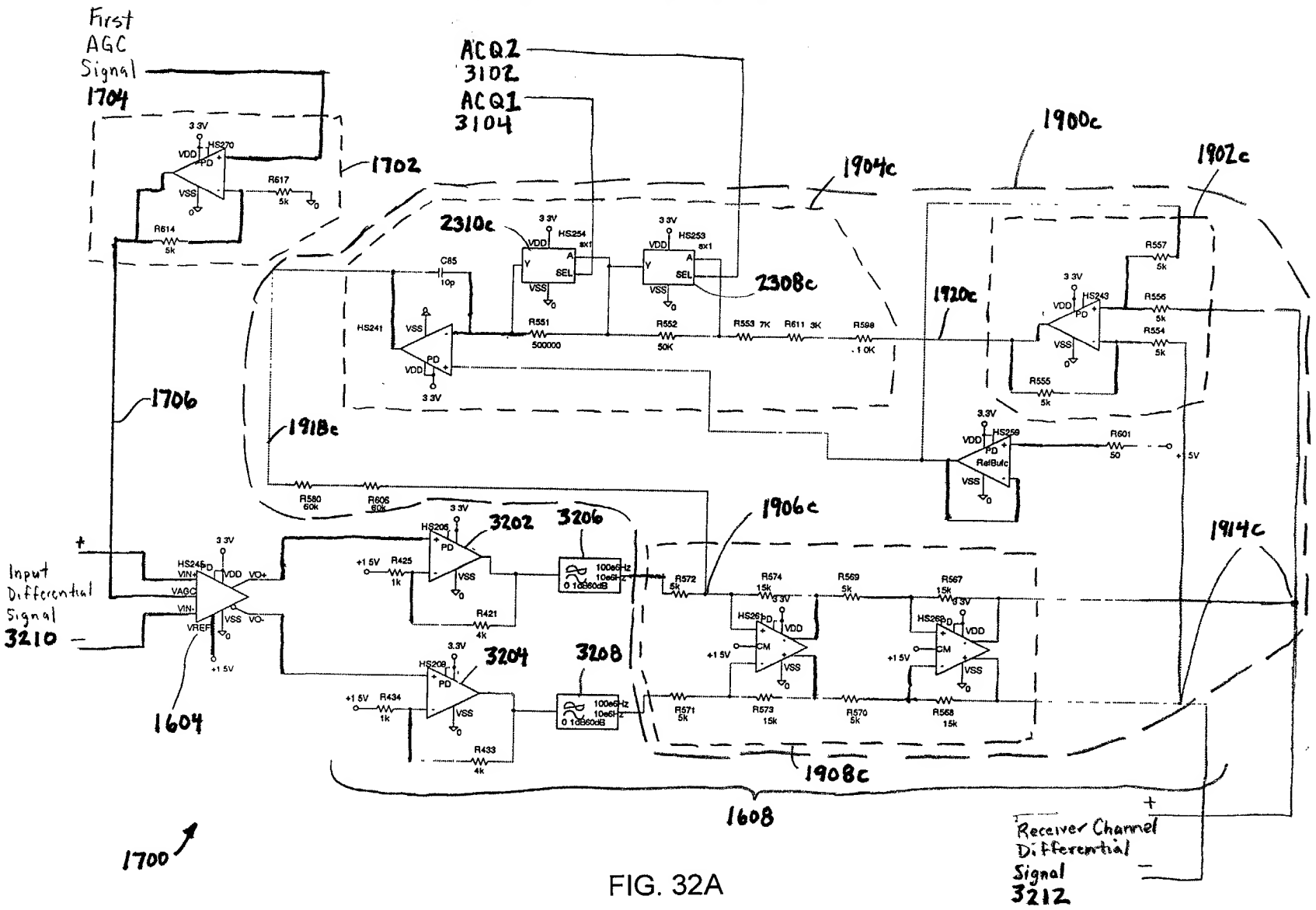

FIG. 32A

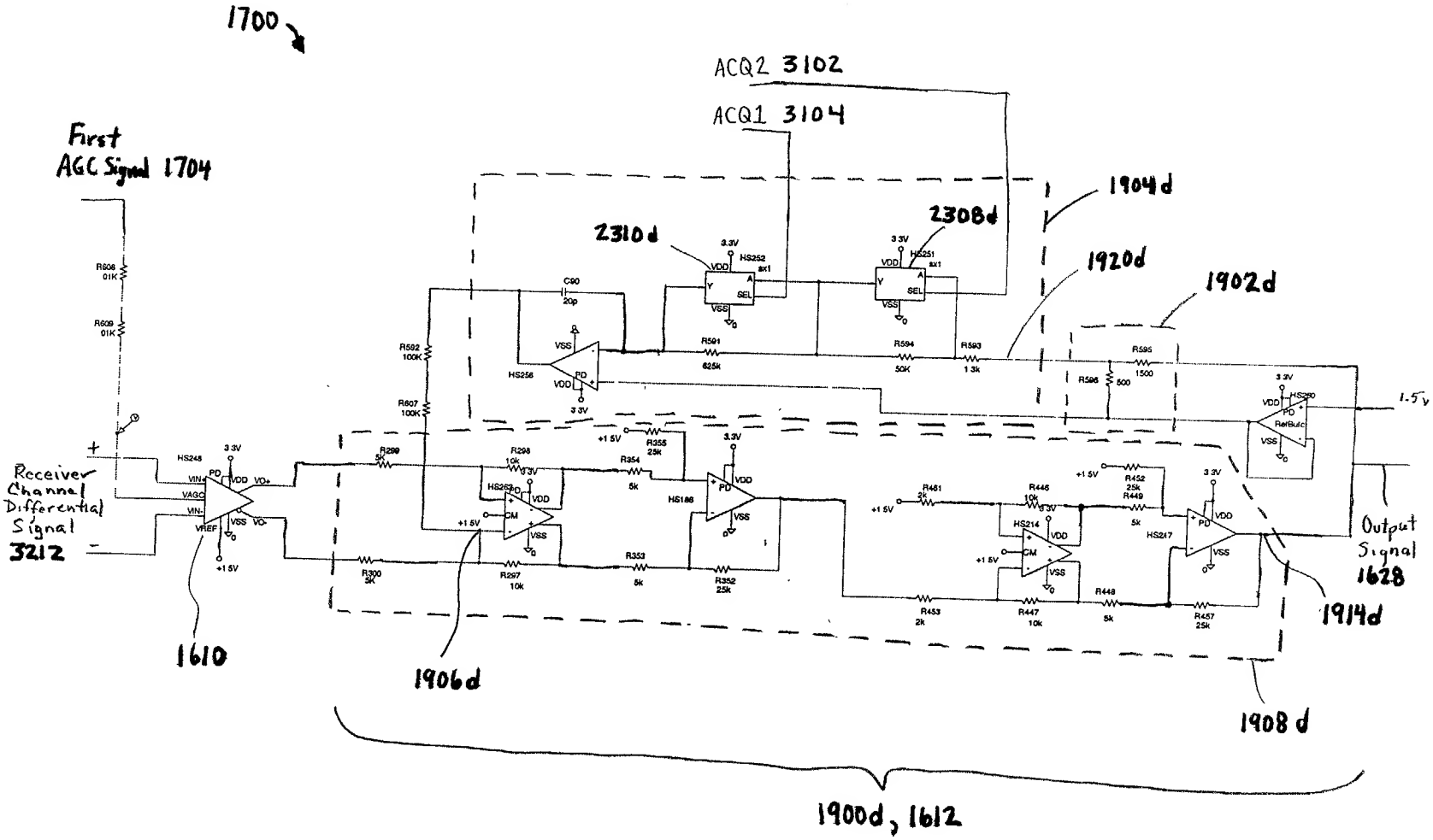

FIG. 32B

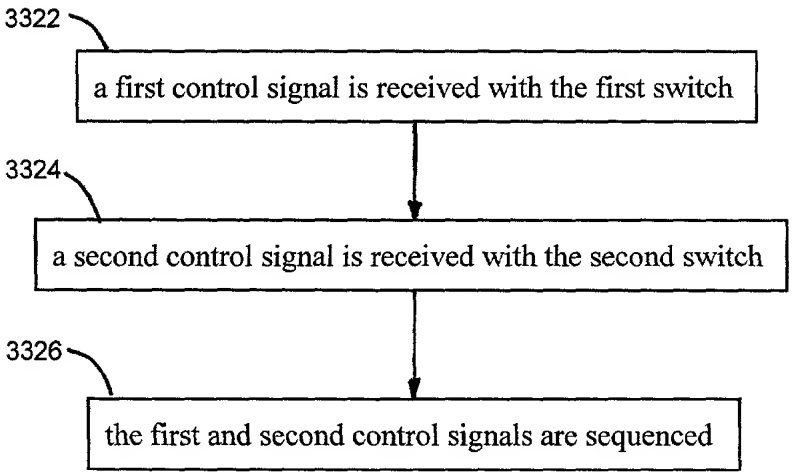
3322
a first control signal is received with the first switch
3324
a second control signal is received with the second switch
3326
the first and second control signals are sequenced

FIG. 33

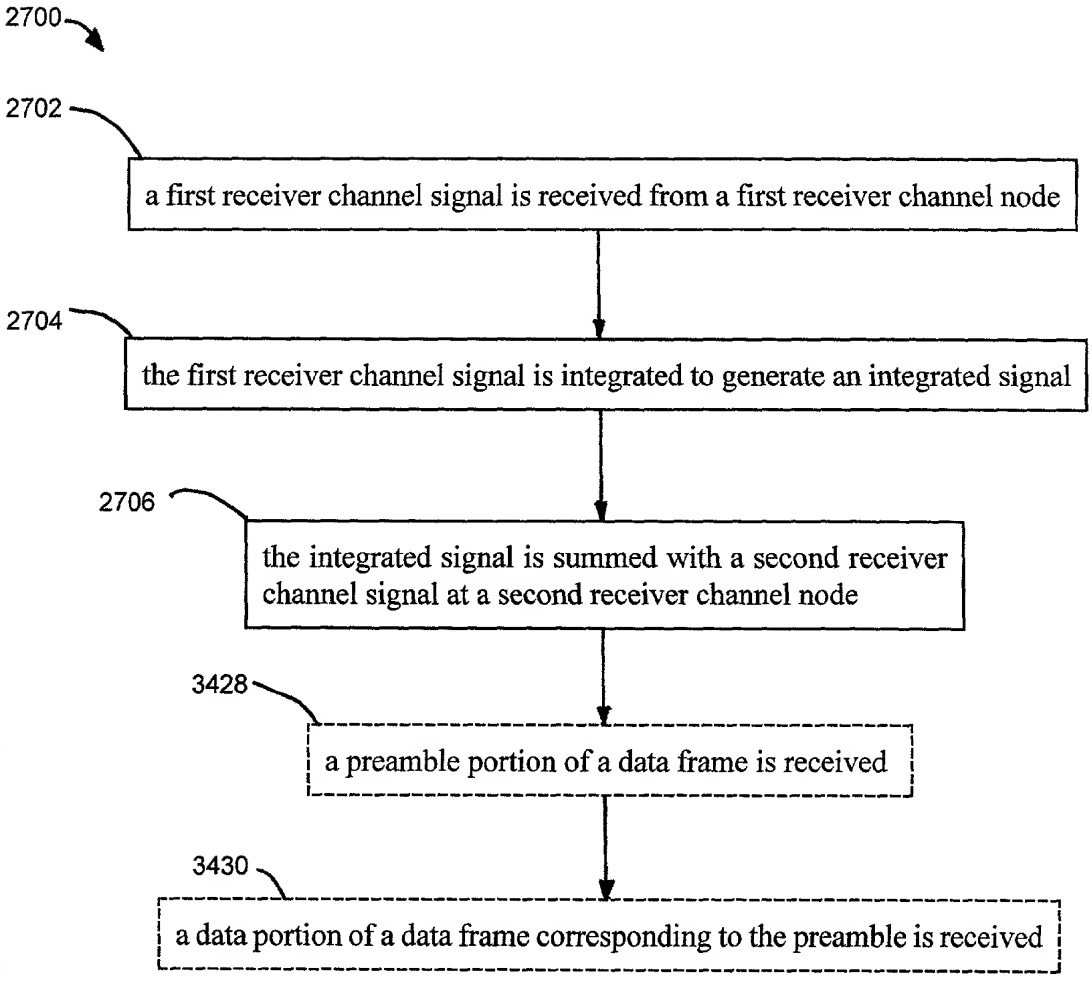
2700
2702
a first receiver channel signal is received from a first receiver channel node
2704
the first receiver channel signal is integrated to generate an integrated signal
2706
the integrated signal is summed with a second receiver channel signal at a second receiver channel node
3428
a preamble portion of a data frame is received
3430
a data portion of a data frame corresponding to the preamble is received

FIG. 34

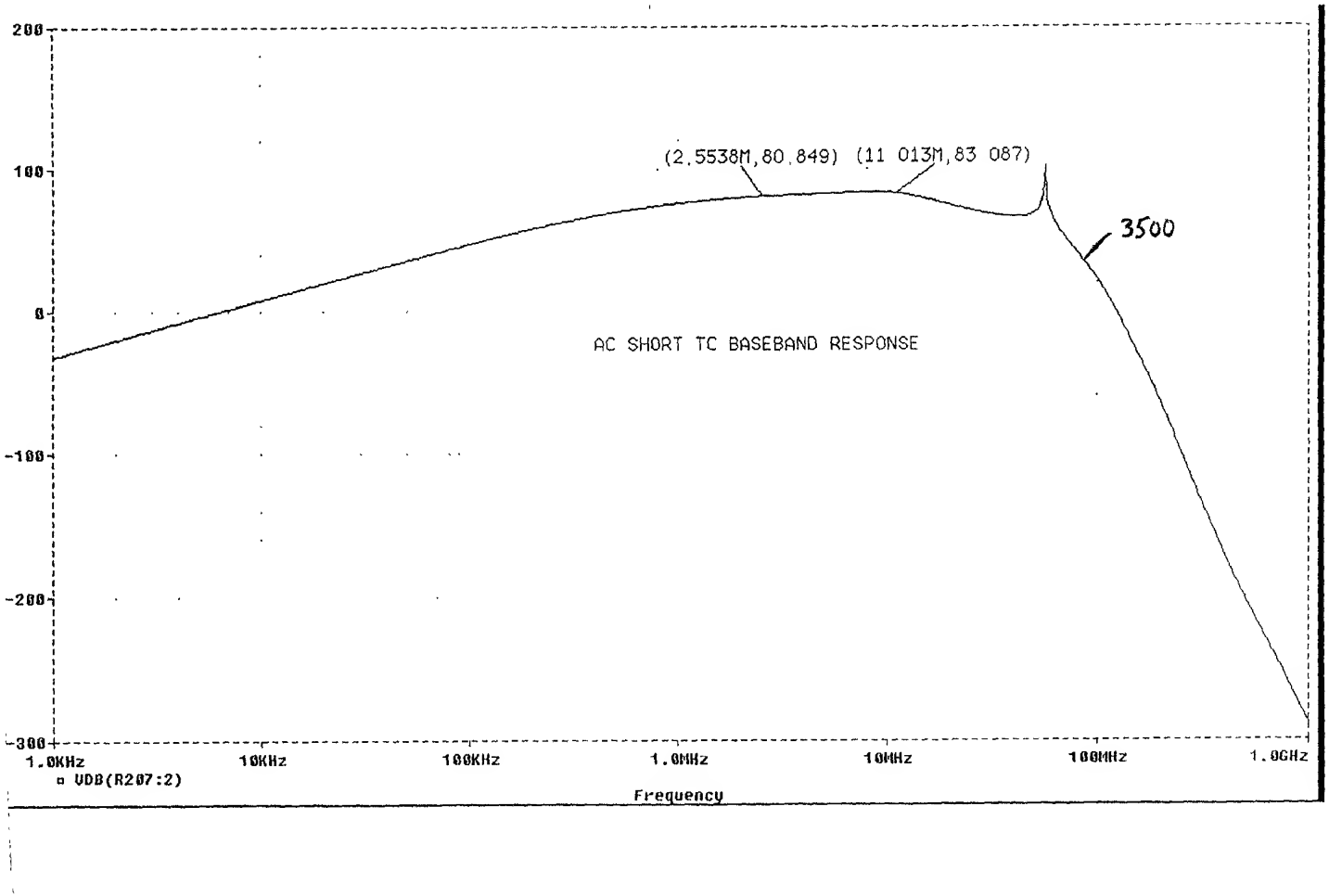

FIG. 35

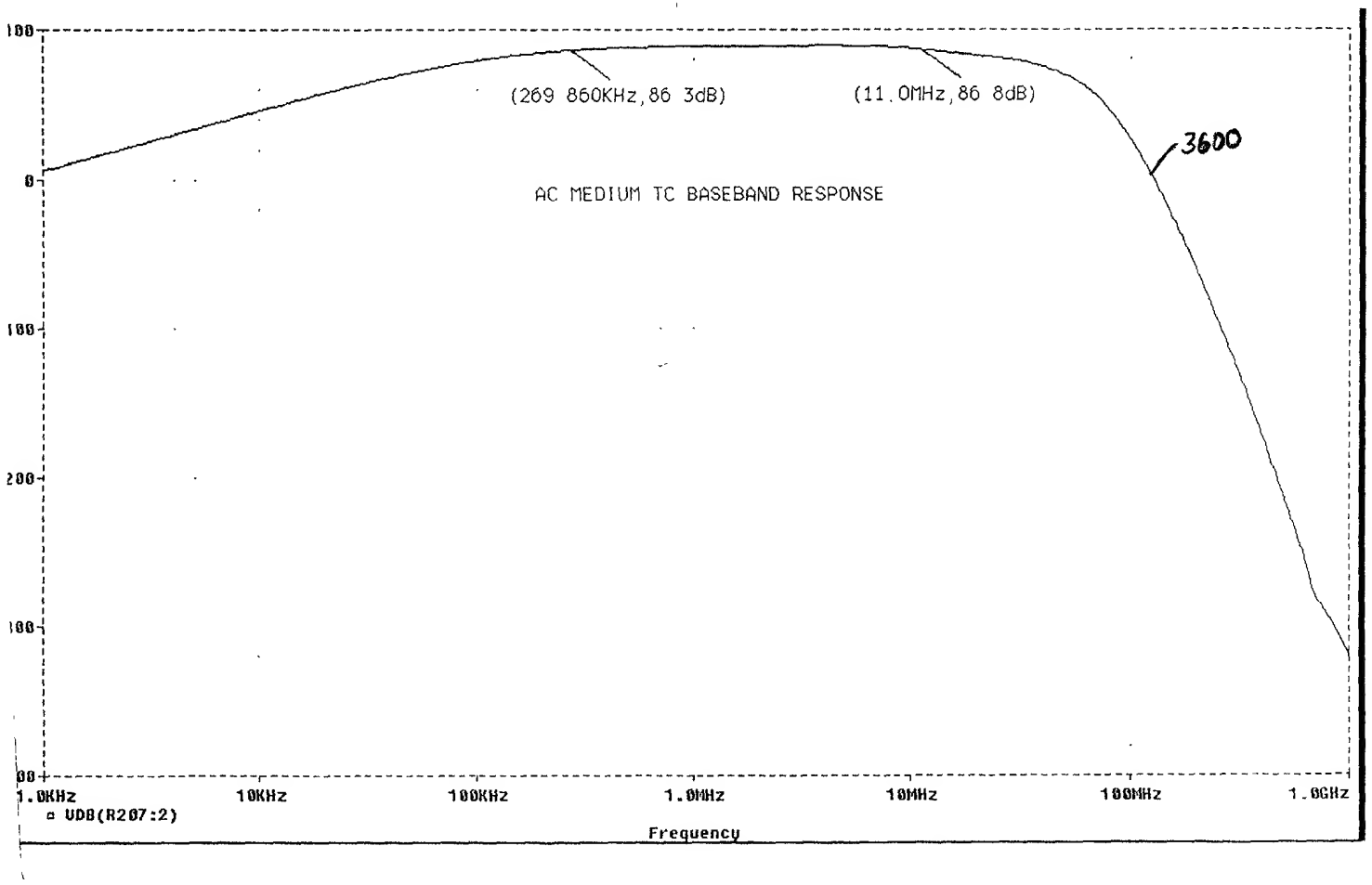

FIG. 36

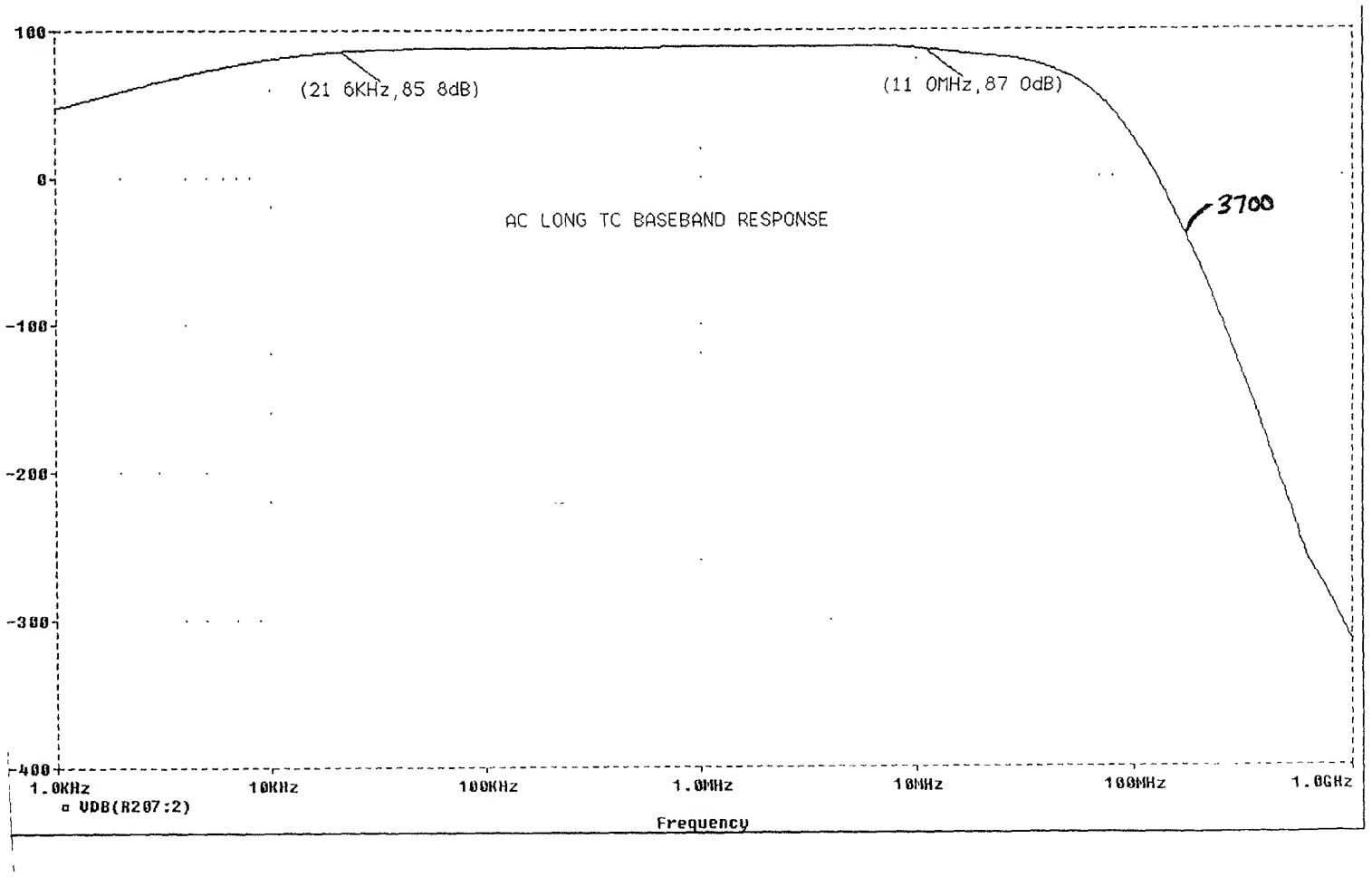
100
0
-100
-200
-300
-400
(21 6KHz,85 8dB)
(11 0MHz,87 0dB)
AC LONG TC BASEBAND RESPONSE
3700
1.0KHz
10KHz
100KHz
1.0MHz
10MHz
100MHz
1.0GHz
VDB(R207:2)
Frequency

FIG. 37

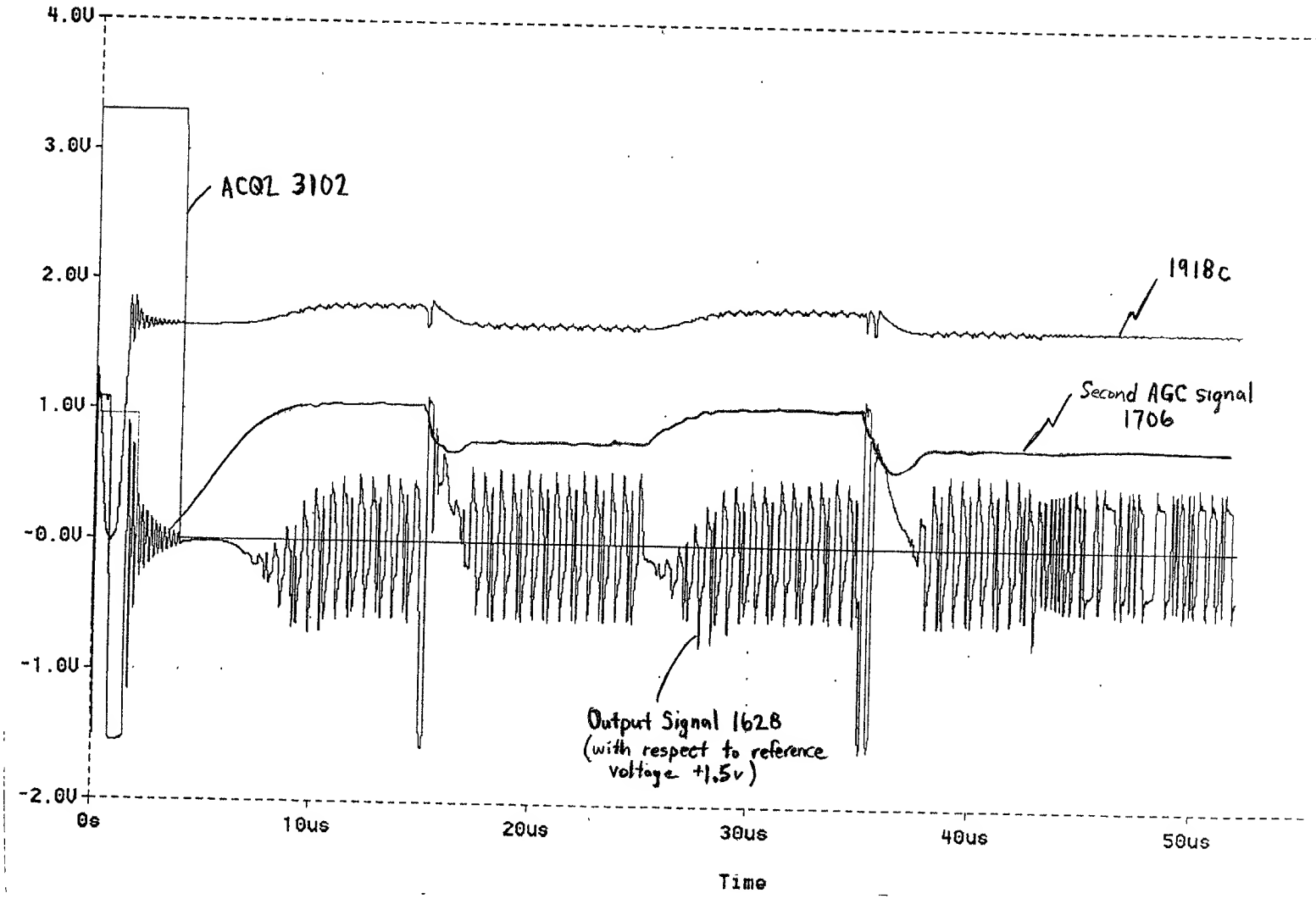
4.0U
3.0U
2.0U
1.0U
-0.0U
-1.0U
-2.0U
ACQL 3102
1918c
Second AGC signal
1706
Output Signal 1628
(with respect to reference
voltage +1.5v)
0s
10us
20us
30us
40us
50us
Time

FIG. 38

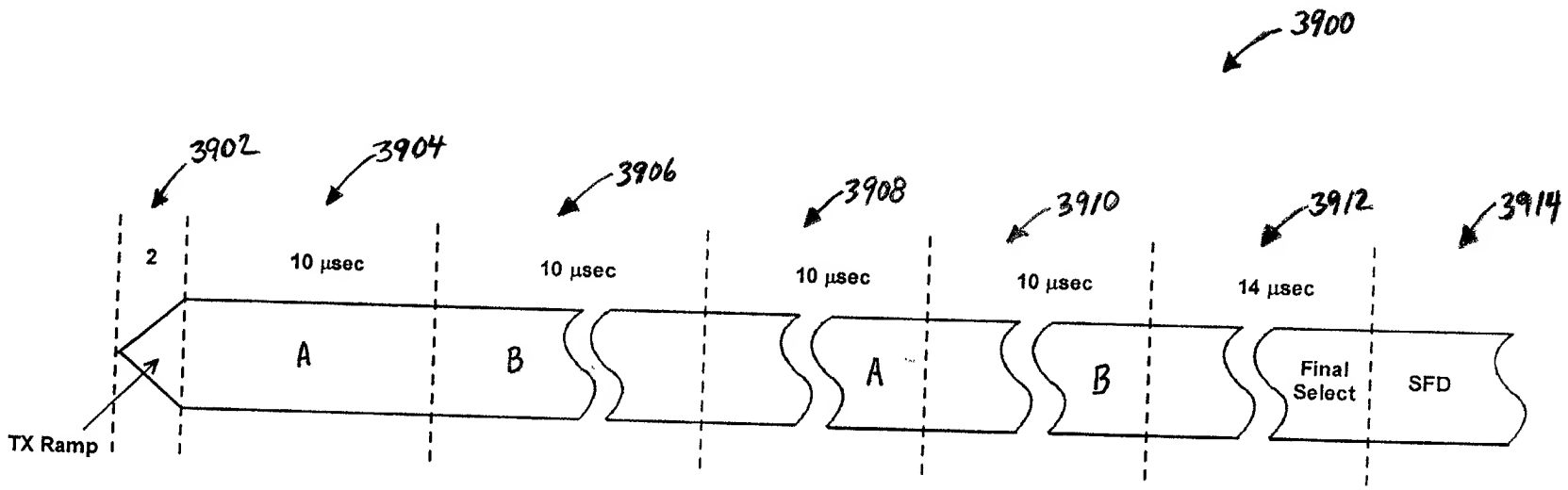

FIG. 39

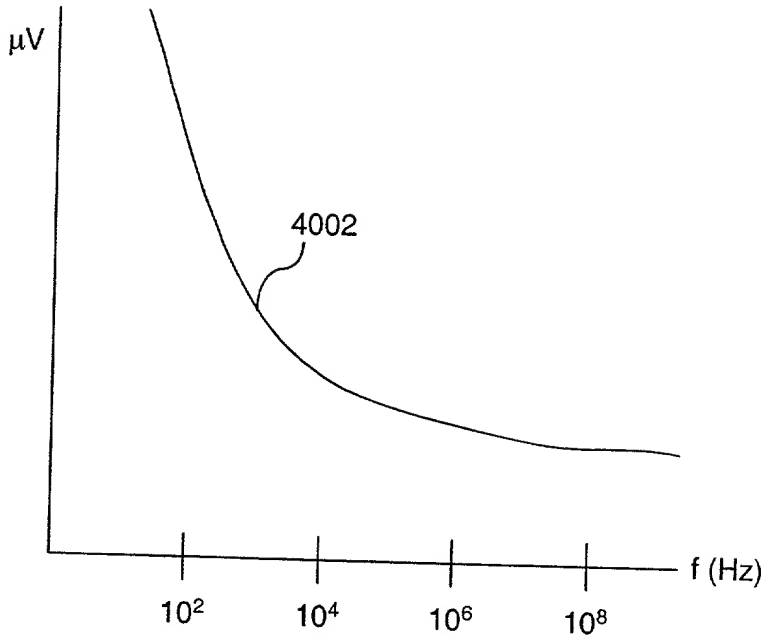
μV
4002
f (Hz)
10^2
10^4
10^6
10^8

FIG. 40

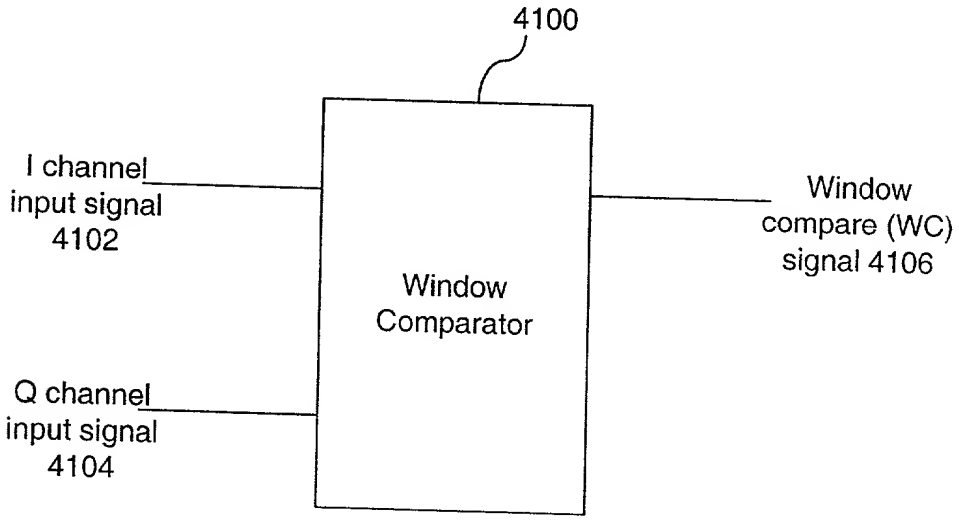
4100
I channel input signal 4102
Q channel input signal 4104
Window Comparator
Window compare (WC) signal 4106

FIG. 41

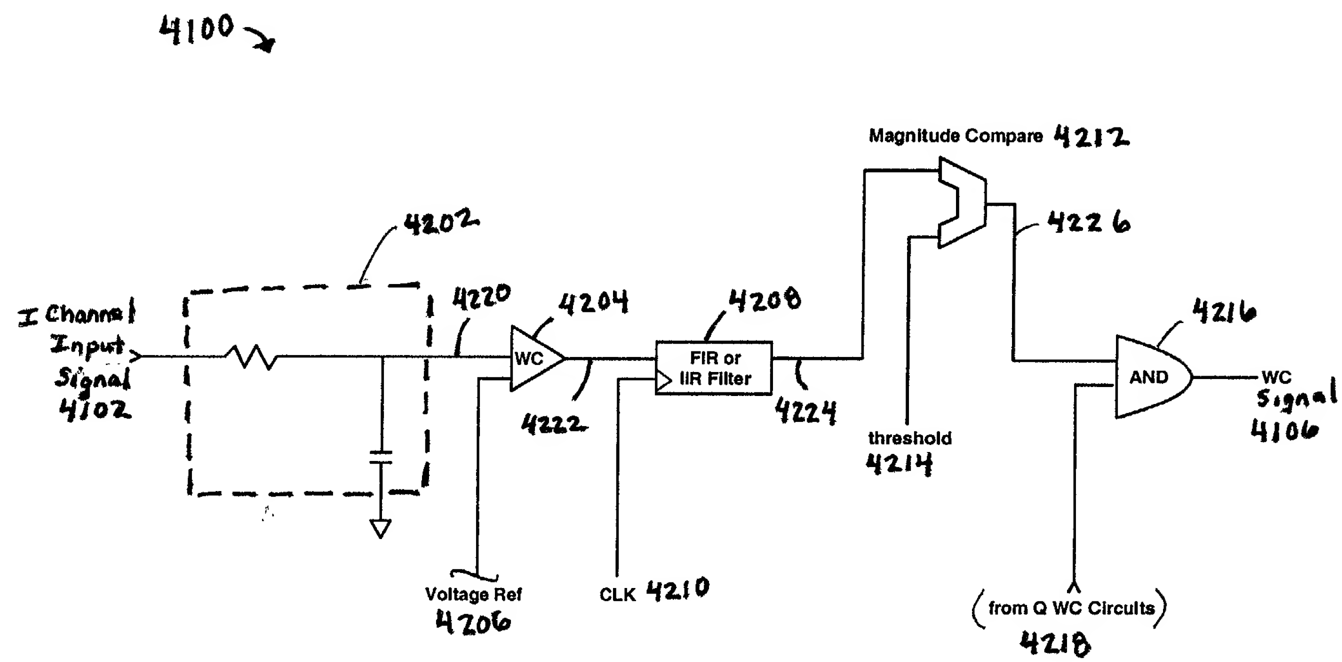
4100
I Channel Input Signal 4102
4202
4220
4204
WC
4222
Voltage Ref 4206
4208
FIR or IIR Filter
CLK 4210
4224
Magnitude Compare 4212
threshold 4214
4226
4216
AND
WC Signal 4106
(from Q WC Circuits) 4218

FIG. 42

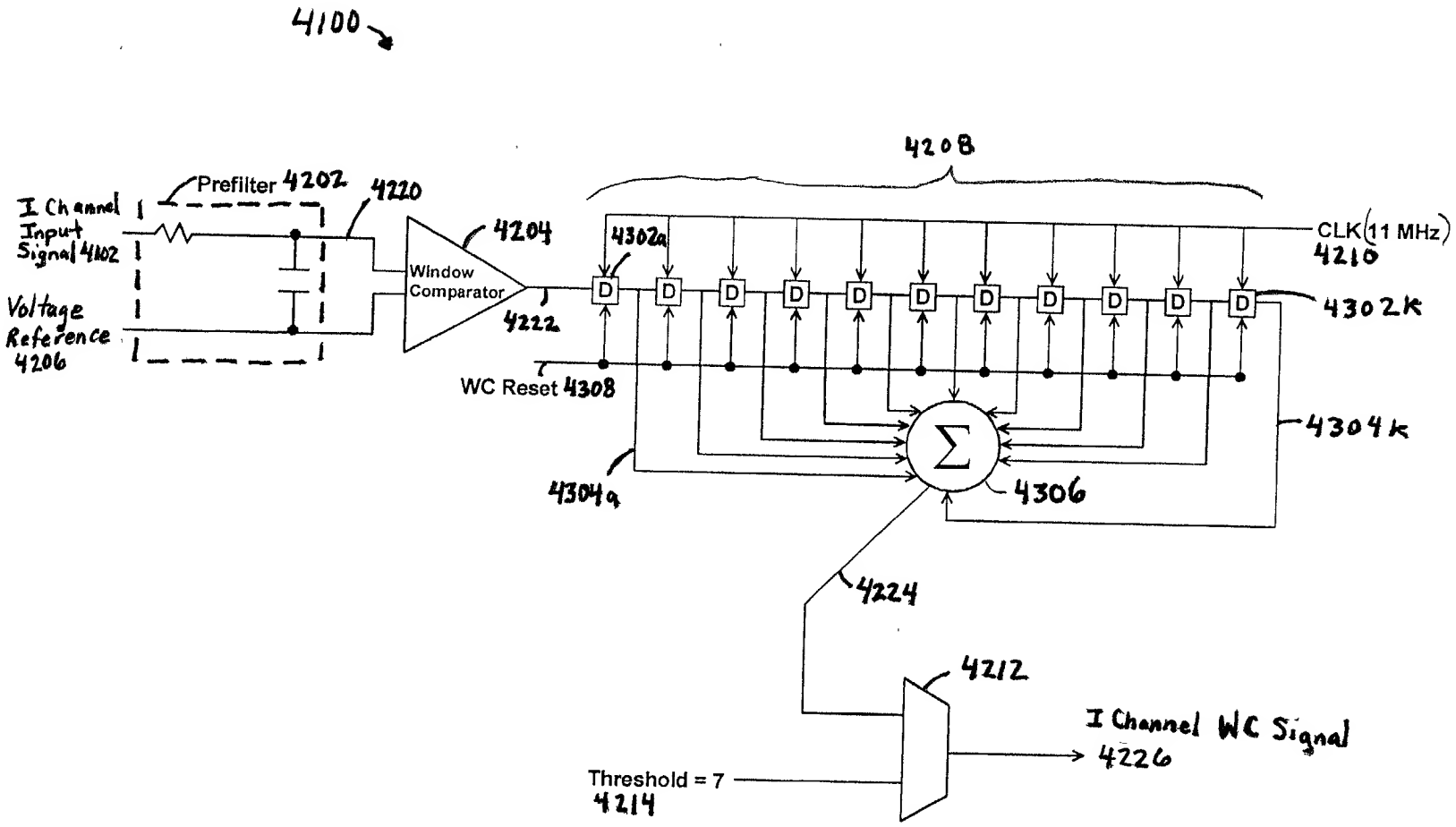

FIG. 43

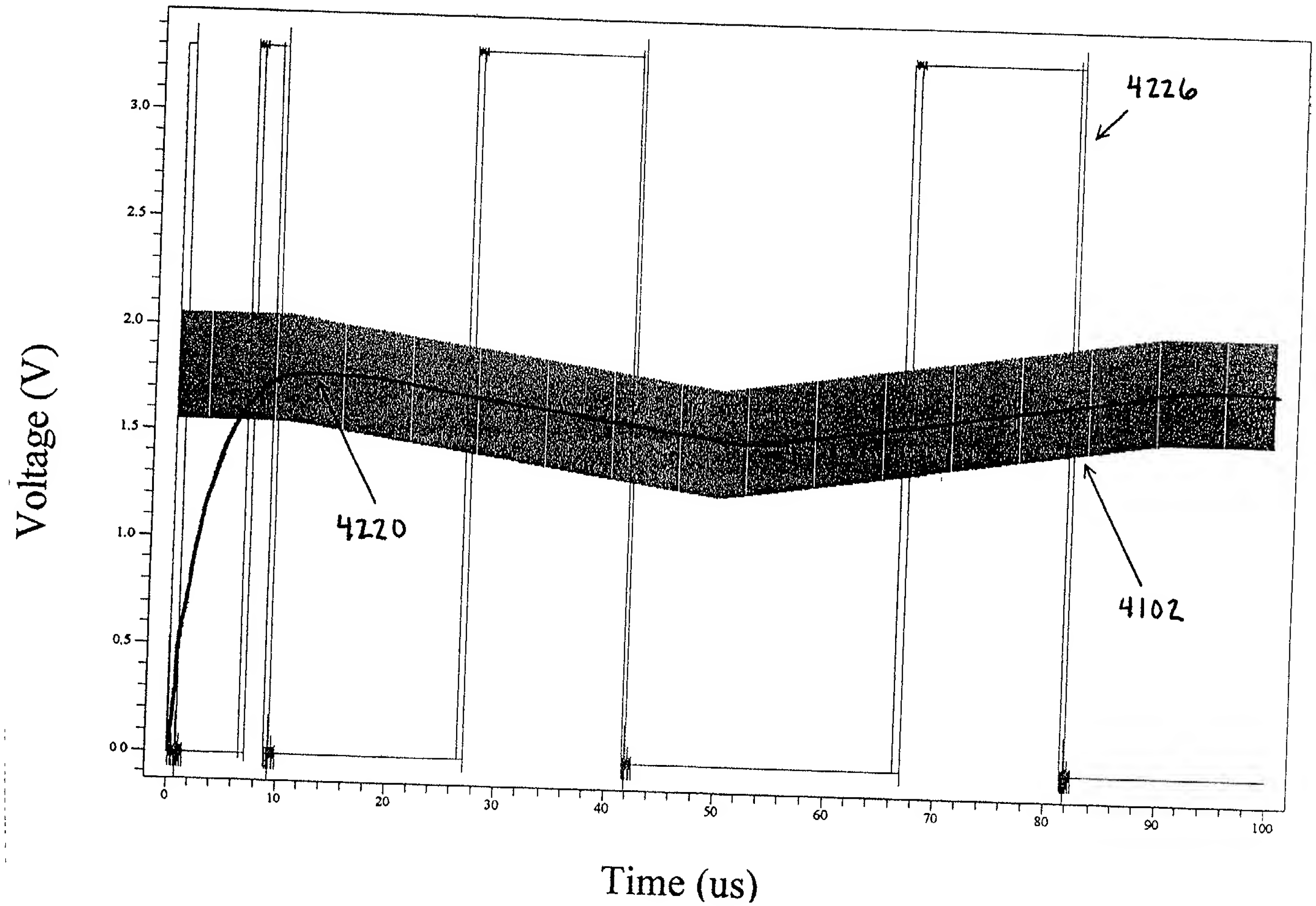
4226
4220
4102
Voltage (V)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
10
20
30
40
50
60
70
80
90
100
Time (us)

FIG. 44

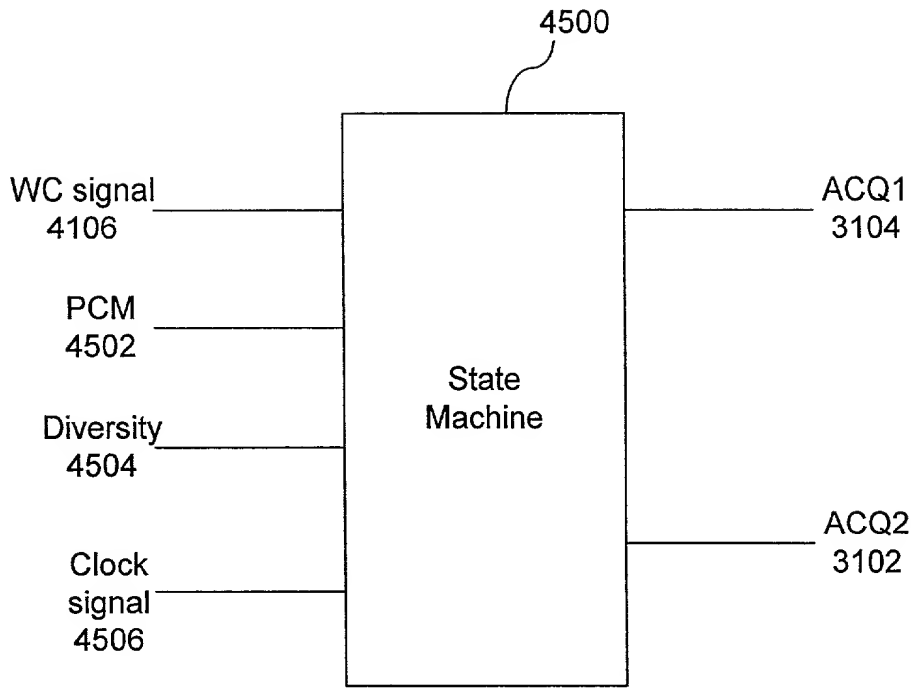
4500
WC signal
4106
PCM
4502
Diversity
4504
Clock
signal
4506
State
Machine
ACQ1
3104
ACQ2
3102

FIG. 45

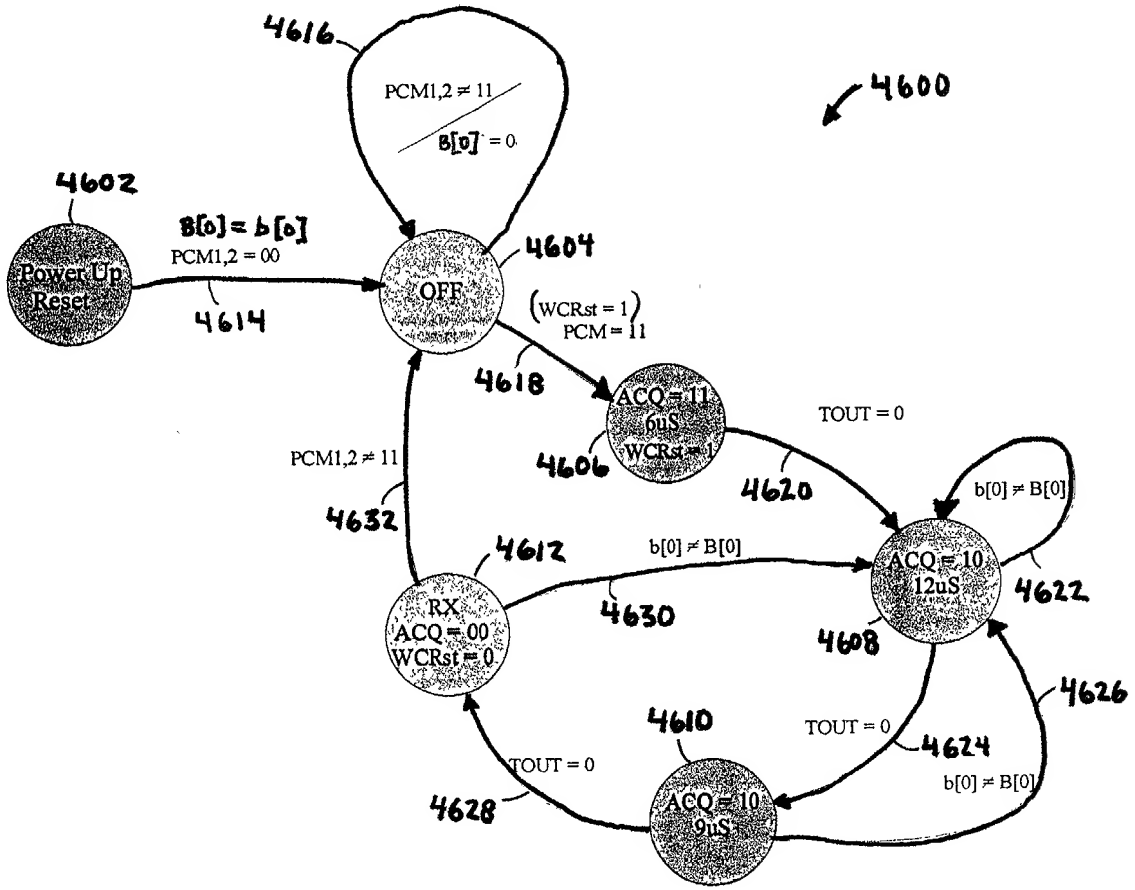
4600
4602
Power Up Reset
B[0] = b[0]
PCM1,2 = 00
4614
4604
OFF
4616
PCM1,2 ≠ 11
B[0] = 0
(WCRst = 1
PCM = 11
4618
ACQ = 11
6uS
WCRst = 1
4606
TOUT = 0
4620
PCM1,2 ≠ 11
4632
b[0] ≠ B[0]
4622
4612
RX
ACQ = 00
WCRst = 0
b[0] ≠ B[0]
4630
ACQ = 10
12uS
4608
4626
4610
TOUT = 0
4624
TOUT = 0
4628
ACQ = 10
9uS
b[0] ≠ B[0]

FIG. 46

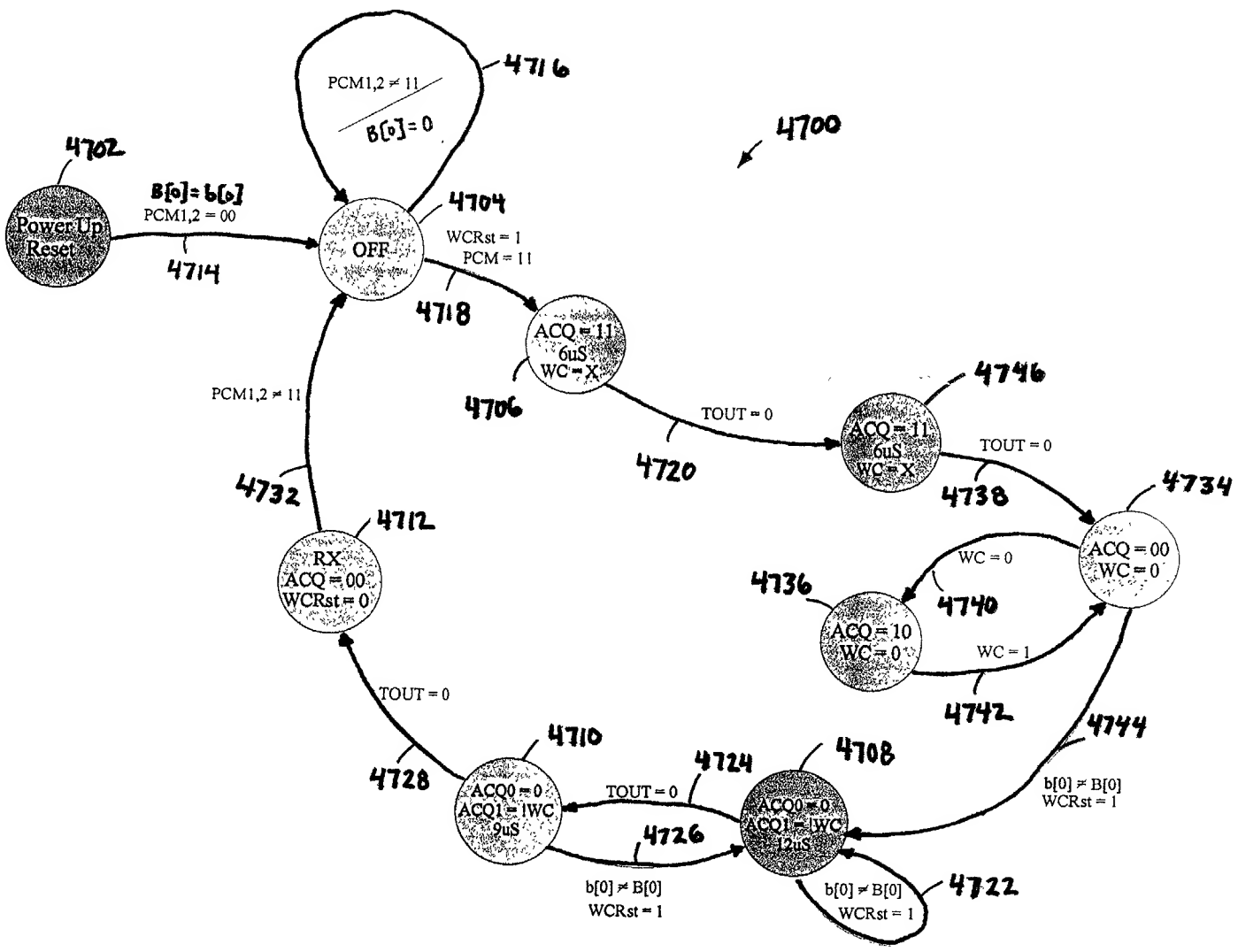

FIG. 47

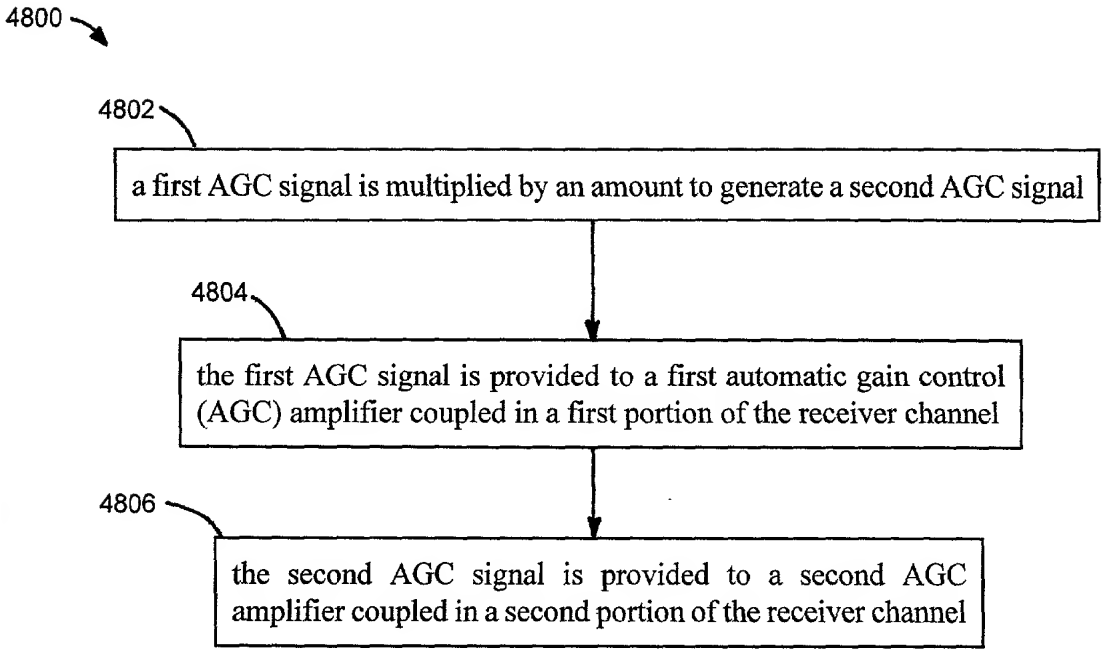
4800
4802
a first AGC signal is multiplied by an amount to generate a second AGC signal
4804
the first AGC signal is provided to a first automatic gain control (AGC) amplifier coupled in a first portion of the receiver channel
4806
the second AGC signal is provided to a second AGC amplifier coupled in a second portion of the receiver channel

FIG. 48

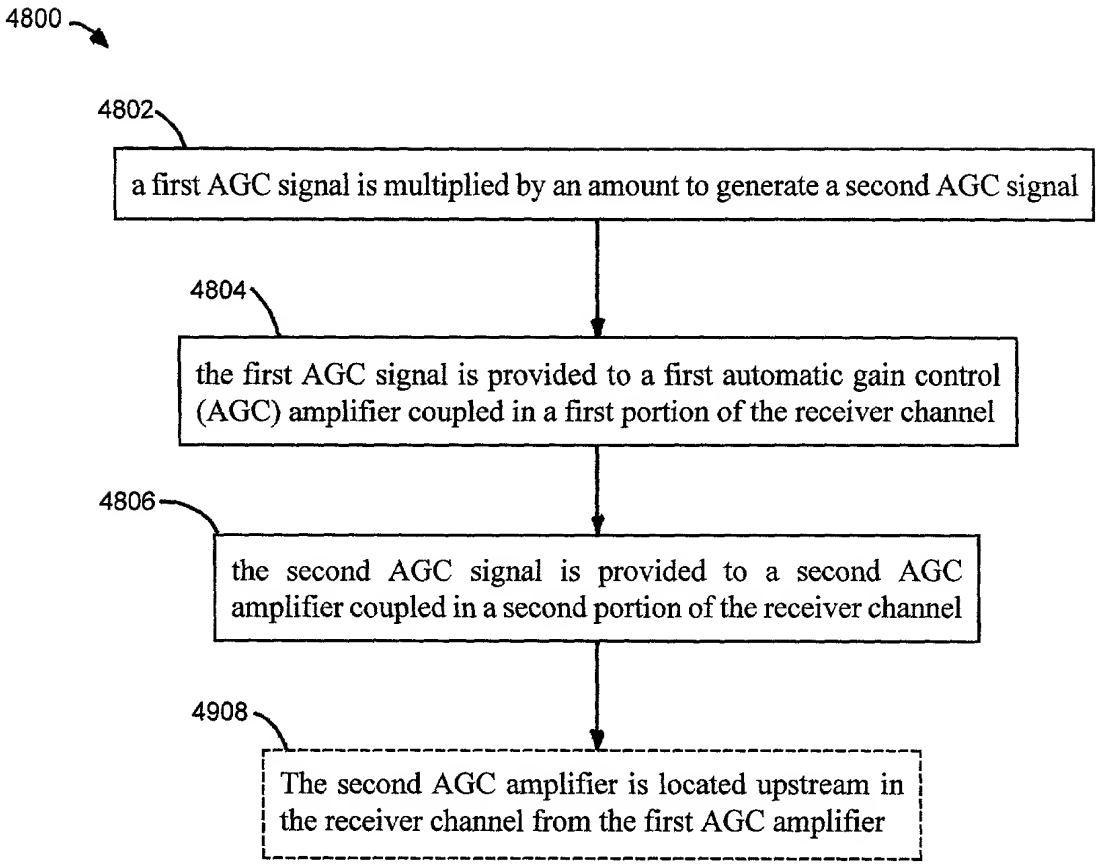
4800
4802
a first AGC signal is multiplied by an amount to generate a second AGC signal
4804
the first AGC signal is provided to a first automatic gain control (AGC) amplifier coupled in a first portion of the receiver channel
4806
the second AGC signal is provided to a second AGC amplifier coupled in a second portion of the receiver channel
4908
The second AGC amplifier is located upstream in the receiver channel from the first AGC amplifier

FIG. 49

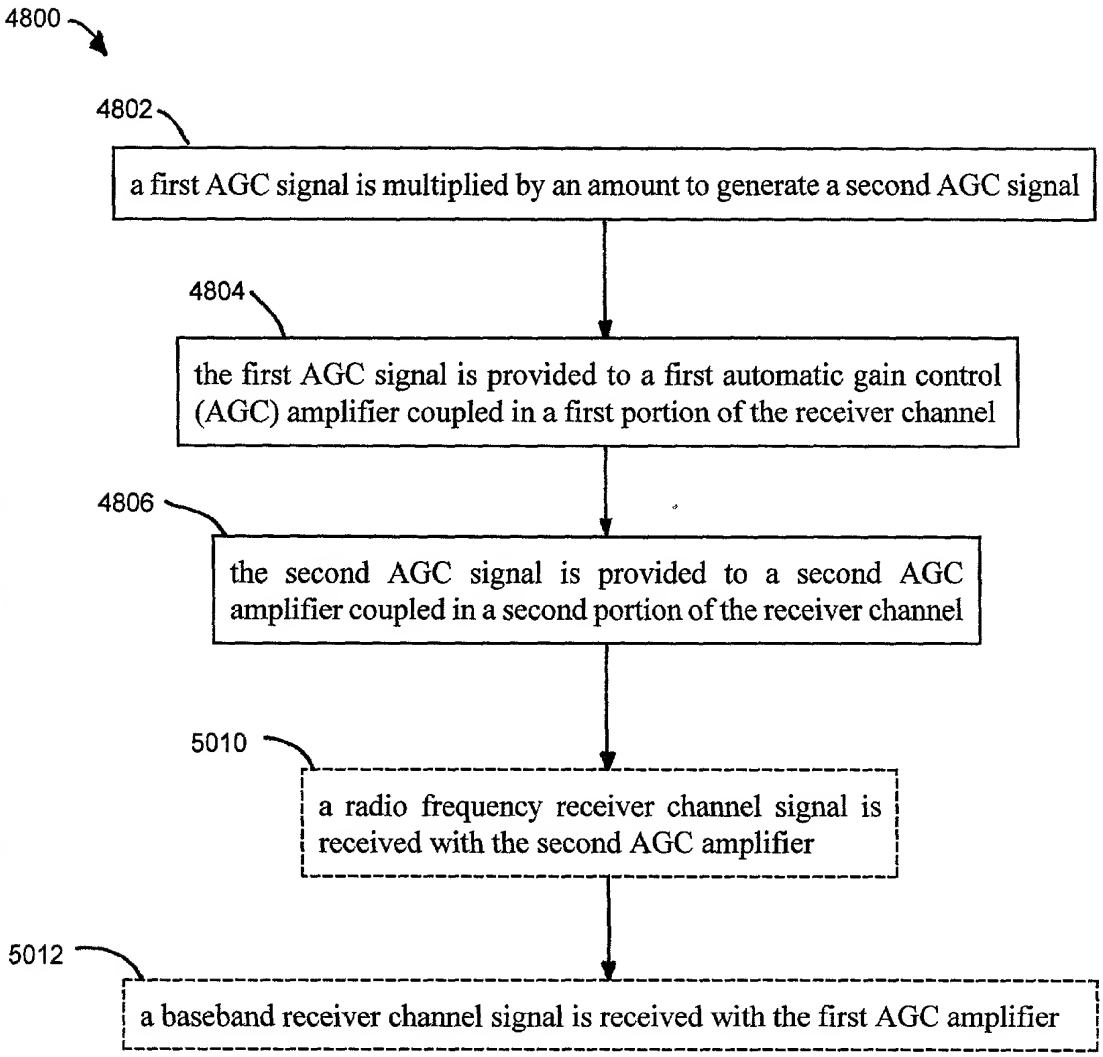
4800
4802
a first AGC signal is multiplied by an amount to generate a second AGC signal
4804
the first AGC signal is provided to a first automatic gain control (AGC) amplifier coupled in a first portion of the receiver channel
4806
the second AGC signal is provided to a second AGC amplifier coupled in a second portion of the receiver channel
5010
a radio frequency receiver channel signal is received with the second AGC amplifier
5012
a baseband receiver channel signal is received with the first AGC amplifier

FIG. 50

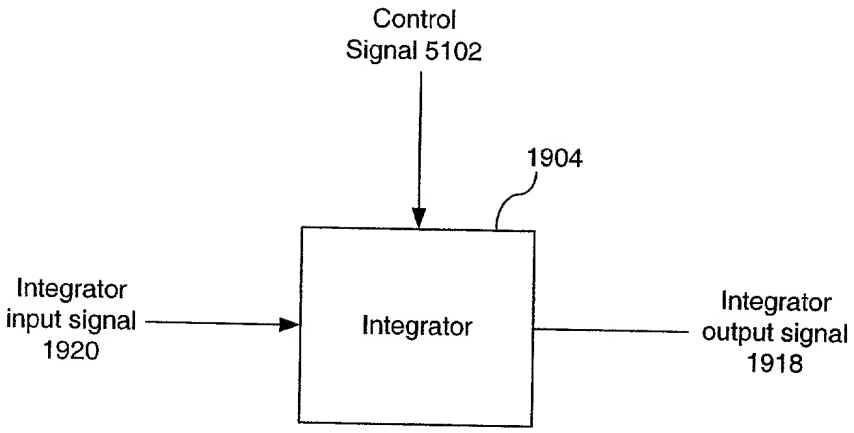
Control
Signal 5102
1904
Integrator
input signal
1920
Integrator
Integrator
output signal
1918

FIG. 51

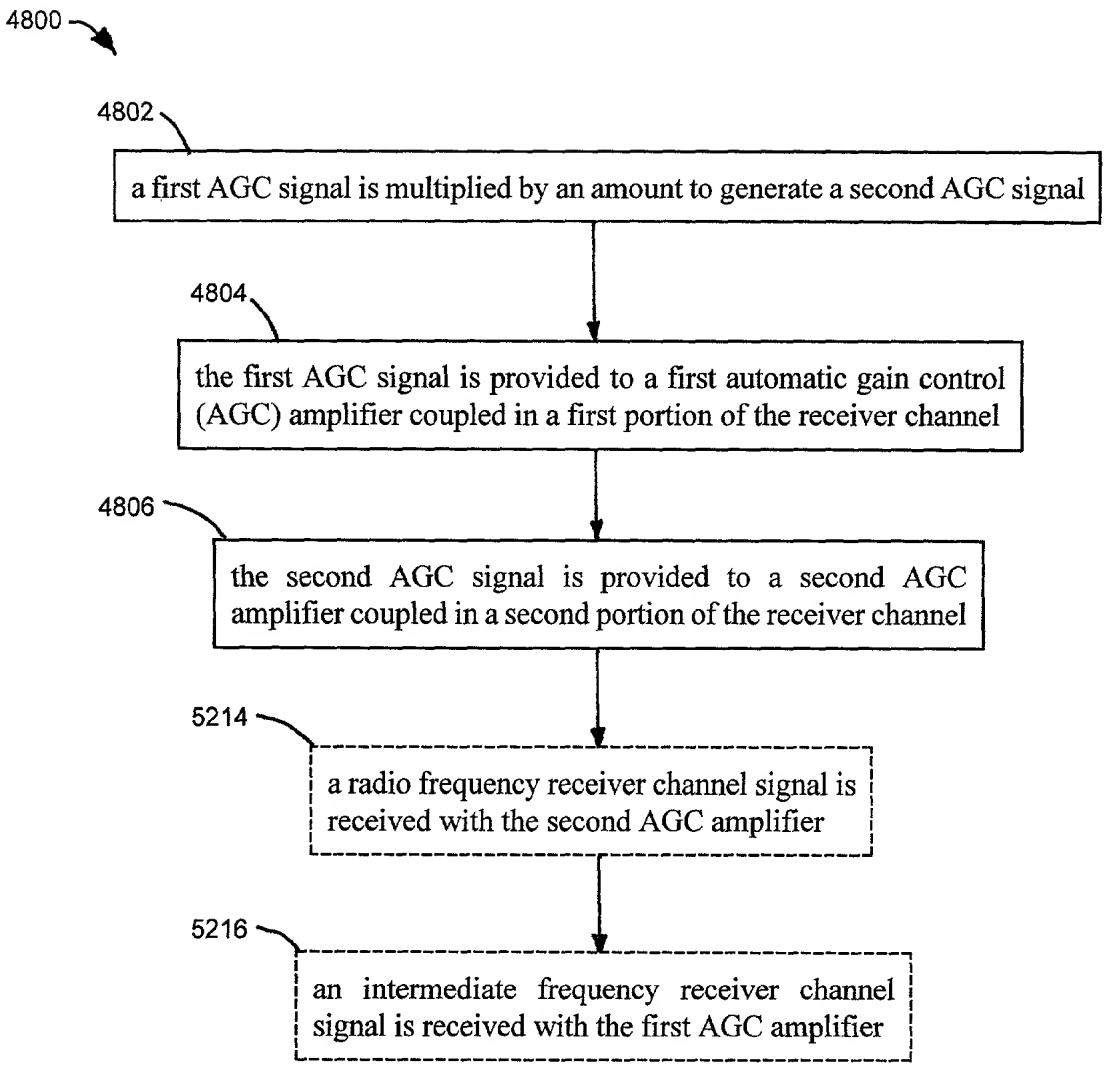
4800
4802
a first AGC signal is multiplied by an amount to generate a second AGC signal
4804
the first AGC signal is provided to a first automatic gain control (AGC) amplifier coupled in a first portion of the receiver channel
4806
the second AGC signal is provided to a second AGC amplifier coupled in a second portion of the receiver channel
5214
a radio frequency receiver channel signal is received with the second AGC amplifier
5216
an intermediate frequency receiver channel signal is received with the first AGC amplifier

FIG. 52